Real-Time Digital Baseband System for Ultra-Broadband THz Communication

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***Abstract*—The research in communications at sub-THz and THz frequencies is currently confined to static wireless links due to the bottlenecks in interfacing with the real-time digital back-ends. A software defined radio platform to support real-time ultra-broadband communications over multi-GHz bandwidths at THz frequencies is proposed. A prototype for the transmit-side is implemented and experimentally demonstrated.**

I. Introduction

Data rates of 1 Tbps will be required to satisfy the demand for fast communications. Moving to the 100+ GHz bands is a must. Such bands exploit abundant spectrum having dozens of contiguous bandwidth for future needs. Wireless at both sub-THz and THz with multi-GHz bandwidths was previously explored from a theoretical standpoint. Recent experiments demonstrated the feasibility of such links albeit using off-line processing [**?**], [**?**]. Advancing to a real-time software defined radio (SDR) platform with sufficient adaptability to support the development and testing of custom-designed physical layer solutions at sub-THz and THz bands leads to uncharted engineering challenges that stem from both the cost and complexity in digital to analog (DAC) as well as analog to digital converters (ADCs) operating around 10-100 GSps.

One approach for realizing ultra-broadband signals with digital backends would be to use data links consisting of multiple frequency multiplexed radio channels, each supporting a slower data stream using manageably small bandwidth. Each low-bandwidth channel is processed on its own backend leading to a multirate baseband SDR processor. Having multiple ADC/DAC chips interfaced to an SDR is an impractical approach due to prohibitive hardware complexity and power consumption. We propose a solution where a system-on-a-chip (SoC) with multiple data converters (which can support at least few GSps of sample rates per converter) are integrated on the same chip alongside a reconfigurable SDR. We exploit Xilinx radio-frequency SoCs (RFSoCs)—an outcome of DARPA's radio frequency field programmable gate array RF-FPGA Program—to enable low size-weight-and-power realization of multi-channel frequency multiplexed SDR.

II. Proposed System and Prototype Implementation

Xilinx RF-SoCs contain multiple (e.g., 8×8 in the ZU28R chip) DACs/ADCs alongside the programmable logic fabric [**?**]. The RFSoCs are typically used for phased arrays for 5G mmWave applications [19], [20]. Here, we leverage the RF-SoCs to parallel-process frequency-multiplexed multi-GHz-wide channels using the on-chip multiple data converters for sub-THz and THz SDR applications.

The transceiver architecture that realizes the proposed methodology is shown in Fig. 1. The transmitter-side architecture, shown in Fig. 1(a), utilizes the DACs in RF-SoCs to generate multiple analog baseband streams. The in-phase/quadrature (IQ) data streams of each baseband channel, is then up-converted to a unique intermediate frequency (IF) to form a frequency-multiplexed aggregated IF signal. This can be achieved through a set of IQ-mixers. Each IQ mixer will upconvert a baseband channel to a different IF carrier $\omega_k,\ k \in \{1, 2, 3, 4\}$, where 2 GHz $< \omega_k <$ 18 GHz. The ω_k frequencies can be carefully picked to ensure sufficient guard between the channels and minimize inter-channel harmonic distortions. Each upconverted IF channel will then be combined using a wideband combiner to form the aggregated IF that will be connected to the radio (sub-THz/THz) front-ends. Similarly, multiple RFSoC systems can be used to aggregate more bandwidth in to the transmission link.

The envisioned receiver-side architecture for real-time processing of the aggregated frequency multiplexed transmission is shown in Fig. 1(b). The receiver circuit architecture, reciprocal to that of the transmitter, demultiplexes the aggregated channels by first splitting the received IF in to number of channels aggregated and then employing a set of IQ-mixers to downconvert each frequency band to baseband for digital SDR processing.

As a proof-of-concept, we have engineered the transmitter-side using the Xilinx ZCU111 board that features the ZU28DR RFSoC chip. This chip supports eight DACs and ADCs that can be clocked at a max rate of 6.55 GSps and 4.096 GSps, respectively supporting a total bandwidth of 26.2 GHz at the DACs and 16.4 GHz of bandwidth at the ADCs. The DACs in the ZU28DR RFSoC chip support 14-bit where as the ADCs are of 12-bit resolution.

For the prototype design of the transmitter-side, minimum of maximum clockable frequencies at both DACs and ADCS, which is 4.096 GSps is used. In order to relax the analog filtering requirements of anti-imaging and anti-aliasing filters, $2\times$ interpolation/decimation is used at DACs and ADCs, respectively. Figure 1(c) shows the prototype setup of the implemented Xilinx RFSoC based back-end system. Here, 2 DACs are used to generate/process a single (complex baseband, I and Q separately) 2.048 GHz channel at the transmitter. Therefore, a total of 4 such baseband channels can be accommodated to utilize all the datacoverters available in the ZU28DR chip (given that $4\times$ processing logic can fit in to the PL).

The PHY layer for the transmitter implementation is chosen to be orthogonal frquency division modulation (OFDM).

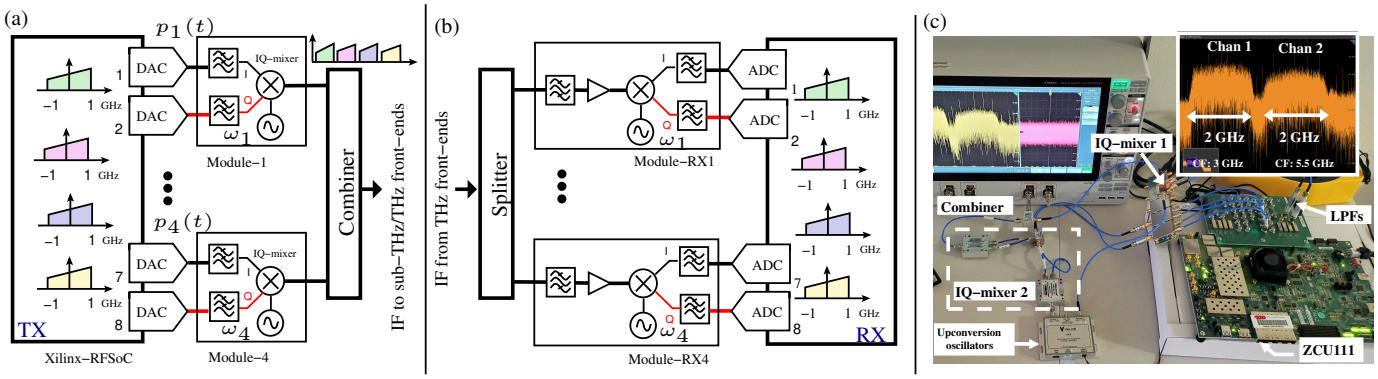

Fig. 1. (a) Overview architecture of the RFSoC-based digital back-end and the IF circuitry at the (a) transmitter-side (c) receiver-side; (c) experimental prototype of OFDM transmitter design multiplexing two 2 GHz channels.

Typically, due to directional nature of the wireless channels at above 100 GHz frequencies, the wireless channel is almost frequency flat but due to the ultrawide bandwidth electronic hardware provides a stronger contribution to the overall channel frequency selectivity. Polyphase digital cores generate orthogonal frequency division multiplexed (OFDM) baseband streams having channel bandwidth 2 GHz. The OFDM implementation uses a 64 subcarrier architecture which corresponds to a subcarrier spacing is 32 MHz. The FFT-size was selected such that frequency response of the electronics is flat across the subcarrier bandwidth for the $\approx$ 2 GHz bandwidth used by each channel. This was done after initial channel gain measurements conducted using 120-140 GHz front-ends available to authors [**?**] (the channel measurements showed that channels can be regarded frequency flat for bandwidths $<$ 50 MHz). The digital cores have been designed to support conventional modulation schemes, namely, BPSK, QPSK, 16-QAM and 64-QAM modulations with the option for control of modulation at the subcarrier-level. Due to the choice of 64-point FFT size, the PHY layer frame structure has been implemented to mimic the IEEE 802.11a standard. Although the DACs and ADCs of the RFSoCs can support sample rates exceeding 4 GHz, the maximum clockable frequency of the PL processing digital circuits are generally bounded at an order of magnitude less than the maximum sampling rates. Therefore, all the digital processing circuits implementing the PHY layer have been designed in a polyphase manner which allows processing of such high data rates from the data-converters.

III. Results

Figure 1(c) shows the experimental setup where two channels, each having 2.048 GHz of bandwidth are combined to form an IF output of 4.096 GHz aggregated bandwidth. The LO frequencies for the two IQ mixers are set to $\omega_1 = 3$ GHz and $\omega_2 = 5.5$ GHz and thus the two transmit channels are centered at 3 GHz and 5.5 GHz. The two-channels were combined using a 2-way combiner and the combined transmitter IF output is shown in the top-right corner of Fig. 1(c). This system is currently being extended to 4 baseband channels to support 8 GHz of bandwidth at the transmitter side leveraging all 8 DACs of the ZU28DR chip. RFSoC based receiver-side processing node will have a similar architecture to demultiplex multi-channel bandwidth and to bring them back to baseband using a set of IQ mixers. Its implementation is saved for future work. The transmitter implementation was verified by sending BPSK modulated data on all data-field subcarriers in channel-1 and QSPK modulated data on all data subcarriers at channel-2. The combined frequency multiplexed IF output was then captured in a digital storage oscilloscope and then the recorded samples were software-processed to obtain the symbol constellations at each channel. Fig. 2 shows the software processed output constellation diagrams for both BPSK an QPSK modulated data, thus verifying the proper transmission of frequency multiplexed aggregated output IF signal.

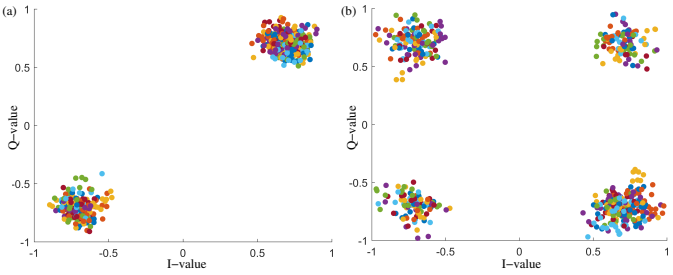

Fig. 2. Software processed output constellations for (a) channel-1 (BPSK modulated data symbols, error vector magnitude [EVM]: -19.5 dB), (b) channel-2 (QPSK-modulated data symbols, EVM: -17.2 dB).

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