



A versatile experimental testbed for ultrabroadband communication networks above 100 GHz

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ABSTRACT

Communication at terahertz (THz) frequencies is envisioned as a near-future landmark in wireless networking and a key component of the sixth generation (6G) wireless systems and beyond. In the last decade, major progress has happened in terms of device technology development as well as THz-wave propagation and channel modeling. In order to advance THz communication and networking research, there is tremendous necessity in developing programmable software-defined hardware and architectures that operate at THz frequencies and are able to process signals with tens to hundreds of GHz of bandwidth, thus making most out of moving to THz band. This paper presents a versatile testbed for conducting wireless experimental research above 100 GHz. The platform consists of multiple sets of analog front-ends at three different frequencies between 100 GHz and 1 THz as well as three different digital signal processing back-ends, able to manipulate more than 10 GHz of bandwidth in real-time. Implementation details and early experimental results to demonstrate the platform capabilities are presented.

1. Introduction

The proliferation of the millimeter wave (mmWave) frequency bands for wireless communications in the fifth generation (5G) mobile networking systems has resulted largely in the mitigation of the spectrum scarcity problem experienced in the sub-6 GHz band. For instance, commercial 5G mobile networks that are being deployed in the 24–52.6 GHz bands (Frequency Range 2 in 5G New Radio) as well as wireless local area networks (WLAN) using the 57–71 GHz spectrum promise to deliver user data rates in excess of 20 Gigabits-per-second (Gbps) for the case of mobile broadband and even 100 Gbps for WLAN, respectively. However, the continuous developments of wireless technologies for applications including broadband mobile data communication, augmented reality, cloud robotics, smart health care, wireless internet of things (IoT) and radio-frequency (RF) sensing, among others, has resulted in heightened demands for both lower latency and larger aggregated network throughput. Moreover, the growing demands from the wireless networks in turn necessitate even faster access networks leading to unprecedented throughput requirements in the back-haul system. Whether for front-haul or back-haul applications, wireless networks that support data rates of up to 1 Terabit-per-second (Tbps) are expected to become a reality in the very near future.

One way to achieve such data rates is to move to carrier frequencies above 100 GHz [1,2] making use of the swaths of bandwidth available at (sub) terahertz (THz) frequencies (100 GHz–10 THz), a range that is also known as the sub-millimeter-wave band. Designing systems directly at optical frequencies (infrared, visible or even ultra-violet, 100–750 THz) can be an interesting and valid option; consider for example, some recent developments at Google that aim to provide rural connectivity using optical links based on free-space laser beams [3]. Nevertheless, the THz band already offers a very large bandwidth (one to two orders of magnitude above that of mmWave systems), while exhibiting advantageous propagation characteristics when compared to optical frequency bands, which are susceptible to occlusions from fog, dust, rain and snow, among others.

Multiple efforts can be observed globally for regulating the spectrum above 100 GHz towards 6G research activities. First, it is relevant to note that the spectrum up to 275 GHz is fully regulated and has been allocated by the International Telecommunication Union (ITU) and, correspondingly in the US, by the Federal Communications Commission (FCC) [4]. Within the 100–275 GHz, there are bands assigned to different services, including fixed & mobile communication systems, satellite & space links, amateur radio and scientific bands in which no emission is allowed. Among those allocations, the 122–123 GHz band

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and the 246–248 GHz band have been marked as ISM bands by the ITU. Moreover, in 2019, the US FCC Spectrum Horizons docket [5] enabled access to more bands for unlicensed operation, namely, 116 to 123 GHz, 174.8 to 182 GHz, 185 to 190 GHz, and 244 to 246 GHz bands. This corresponds to freeing up a total of 21.2 GHz of the spectrum for unlicensed operation. In addition, to facilitate and accelerate the exploration and development of new wireless communication and sensing technologies, the FCC created a new category of experimental licenses for the frequencies between 95 GHz and 3 THz. While a step in the right direction, there are still many things to be addressed, including the definition of a much broader contiguous band for ultra-broadband communications and the derivation of more dynamic and spectrally efficient ways to ensure the coexistence of passive users (e.g., Earth exploration satellites and radio astronomers) and active users (e.g., fixed and mobile communications).

Enabling THz communication systems involves overcoming many challenges, which range from the development of transceivers and antennas that can efficiently operate above 100 GHz and the characterization of the wireless channel, to the design of communication algorithms and networking protocols that can make the most of this spectral band. From the device technology perspective, important strides have been made as a result of major recent advancements in electronic, photonic and plasmonic devices [6,7] with corresponding technology demonstrations [8,9]. In terms of propagation characterization, considerable progress has been achieved in the theoretical modeling of THz channels [10,11] and a several measurements of THz channels around 100–300 GHz have been reported [12,13]. Physical layer (PHY) solutions that optimally exploit the THz channel have been proposed [14,15], but with little experimental validations [16]. While network simulation tools exist [17], these are only the first step. Early work on higher layers have been reported in [18,19]. However, to our knowledge, no THz network-level demonstration seems to have taken place.

In light of these facts, there is a tremendous interest in developing reconfigurable, software defined radio (SDR) architectures that support THz frequencies. Moreover, in order to advance wireless communications research at THz bands, SDRs must process digital baseband signals with tens to hundreds of GHz of bandwidth, as needed by emerging 6G networks.

In this paper, we present a state-of-the-art experimental platform for THz communications developed at Northeastern University (Fig. 1) as well as a long-term vision of what is required to fulfill the need. The current testbed covers three key THz frequency bands (namely, 120–140 GHz, 210–240 GHz and 1.0–1.05 THz) with different bandwidths (from 2 GHz to 32 GHz) and is able to perform different functionalities, ranging from propagation and channel modeling to physical layer design and link layer implementation in real-time. For the purpose, various signal processing units are utilized at the back-end to support the required functionality.

In the following sections, we provide a detailed description of the platform. First, in Section 2, we describe the three sets of RF front-ends that integrate the testbed, including their working principle, enabling technology and measured performance. Next, in Section 3, we describe the first of three available digital processing back-ends, namely, an offline ultrabroadband (up to 32-GHz-wide) signal processing engine which offers high flexibility and facilitates the transition from theoretical research to experimental testing. Then, in Section 4, we present a real-time software-defined-radio platform based on the 2 GHz National Instruments (NI) mmWave platform. While the bandwidth of this platform is less than that of the offline engine, it enables the testing of dynamic solutions. Finally, in Section 5, we describe our ongoing work on building a customized real-time multi-GHz multi-channel digital signal processing engine enabled by a state-of-the-art radio frequency system-on-chip (RFSoc), with processing bandwidths greater than 2 GHz (Section 5). For each digital signal processing engine, we provide a summary of the functionalities implemented by

our team and the experimental results conducted to validate the system capabilities.

The purpose of this paper is not to solve a specific research problem in the broad field of THz communications, but to disclose and demonstrate the possibility to conduct all-layers experimental research above 100 GHz. This is a first in this frequency band.

2. Terahertz front-ends

The key capability of a THz communication testbed is its ability to generate, modulate, radiate, detect and demodulate signals at THz frequencies. Our platform has three different sets of THz front-ends that can operate between 120–140 GHz, 210–240 GHz, and 1.00–1.05 THz, depicted in Fig. 2 from left to right, respectively. Despite the different operation frequency, the three sets are based on the same architecture and technology, namely, frequency multiplying, amplifying and mixing chains based on Schottky diode technology [20]. In all the setups, the starting point is also always the same, i.e., a stable multi-GHz sinusoidal signal or local oscillator (LO), in our case provided by identical but separate analog signal generator (Keysight E8257D) at the transmitter and the receiver. As opposed to the majority of experimental platforms for THz communications research, we emphasize that there is no wired synchronization between the transmitter and the receiver. Next, we describe the specifications of each front-end.

2.1. 120–140 GHz front-ends

The 120–140 GHz front-ends are custom-designed by Virginia Diodes Inc. (VDI). The transmitter consists of two frequency doublers, i.e., a total multiplication factor of $\times 4$, to generate the carrier signal starting from a LO signal of 30–35 GHz. Thereafter, a mixer with 7 dB of double sideband conversion loss is utilized to modulate the carrier signal with the information-bearing broadband baseband/IF signal. At RF, a maximum output power of 13 dBm or 20 mw is achieved by an RF power amplifier with 20 dB gain. To down-convert the RF signal to baseband/IF, an identical setup is utilized to generate a THz carrier signal at the receiver side, which is mixed with the received RF signal. In this case, a low noise mixer is utilized to obtain the IF signal. For further amplification of the received signal, a low noise amplifier (LNA) with 12 dB gain is used at the IF stage, given the lack of a LNA at RF.

2.2. 210–240 GHz front-ends

The front-ends at 210–240 GHz have been developed in collaboration with the NASA Jet Propulsion Laboratory (JPL) and leverage NASA's patented multiplier technology based on on-chip power combining [21,22]. The measured output power is a world-record-setting 23 dBm (200 mW) at the given frequency range. The up-converter is based on a $\times 9$ multiplier chain and is used to generate the RF signal from the LO signal of 22.2–26.67 GHz. A high power mixer with 7 dB of conversion loss is utilized to modulate the carrier with the information-bearing signal. The receiver's down-converter is based on a $\times 6$ frequency multiplier–amplifier chain, and with the aid of a mixer, the RF signal is shifted down to the IF range. An IF stage LNA with 35 dB of gain is utilized to provide the required amplification.

2.3. 1.00–1.05 THz front-ends

Similar to the 120–140 GHz system, the 1.00–1.05 THz front-ends are custom designed by VDI. However, these possess a higher-order multiplier chain of $\times 24$ ($\times 2 \times 2 \times 2 \times 3$), which is utilized to generate the carrier from the LO signal ranging between 41.67–43.75 GHz. A sub-harmonic frequency mixer with 15 dB of conversion loss is utilized to modulate the carrier according to the IF signal. The maximum output power of the transmitter front-end is -15 dBm or 30 μ w. At the receiver, an equivalent multiplier chain and low noise mixer with 15 dB of

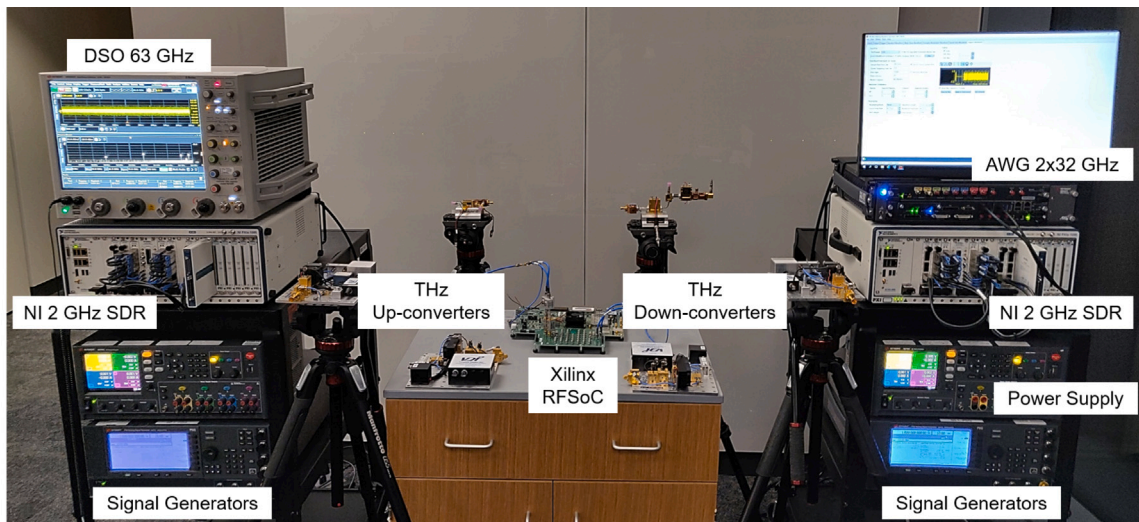


Fig. 1. Ultrabroadband networking systems testbed at Northeastern University.

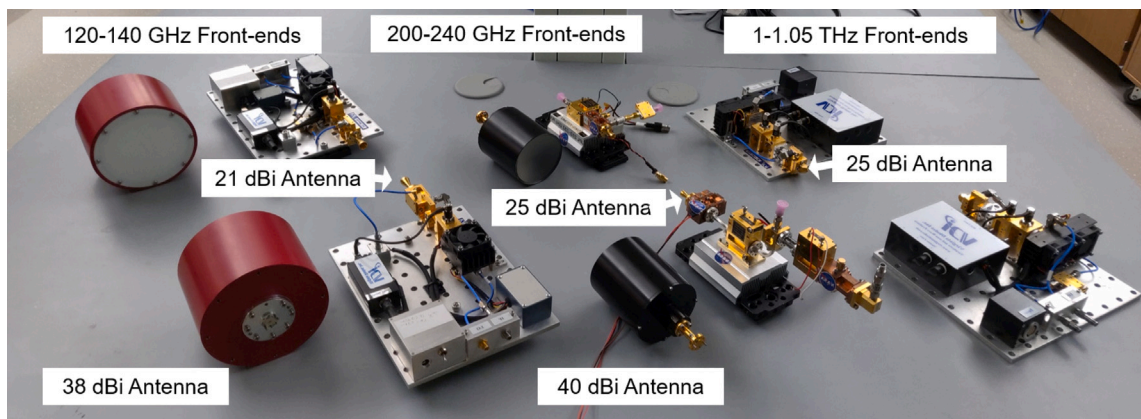


Fig. 2. THz front-ends.

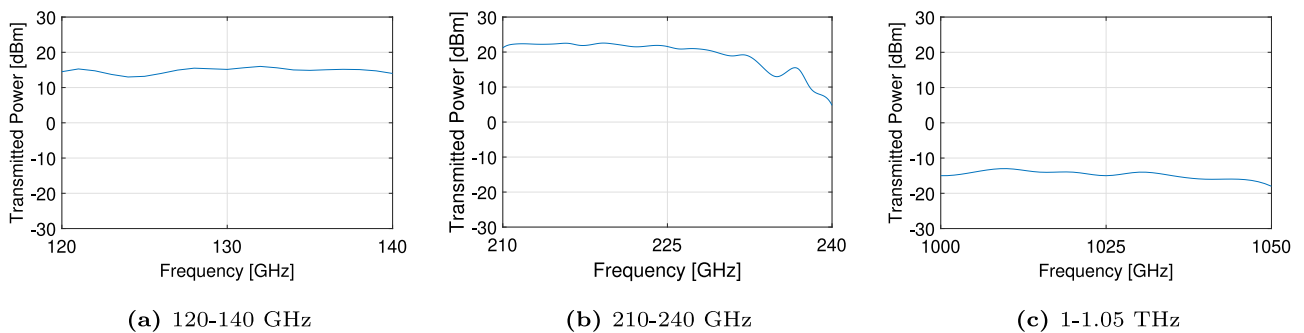


Fig. 3. Maximum transmitted power of the different front-ends within their bandwidth of operation.

conversion loss are employed to obtain the IF signal from the received RF signal. Furthermore, an IF stage LNA with 10 dB of gain is used.

In Fig. 3, we illustrate the maximum transmitted power for the three front-ends within their operational bandwidth to highlight the ultra-broadband nature of the testbed. Furthermore, to exhibit the frequency response of the transceiver system altogether, the received power at 15 m for 120–140 GHz, and 210–240 GHz front-ends with the received power at 15 cm for 1.00–1.05 THz are represented in Fig. 4. The channel frequency characterization is done by generating a constant single tone of 1 GHz with the arbitrary waveform generator (AWG) at the transmitter and sweeping the LO frequency at

the transmitter and the receiver in fixed steps of 1 GHz within the operational bandwidth. Also, we can easily get the receiver side front ends’ frequency-domain behavior by substituting the antenna frequency response and corresponding path loss.

Noise characterization is also an essential step needed to design effective detection algorithms and the required signal processing strategies. The thermal noise in the receiving chain and the absorption noise introduced by water molecules within the channel are the primary sources of noise in the THz band. In our system, the measured noise power spectral density N_0 is $1.9 \times 10^{-17} \text{ W Hz}^{-1}$, $3.6 \times 10^{-16} \text{ W Hz}^{-1}$, and

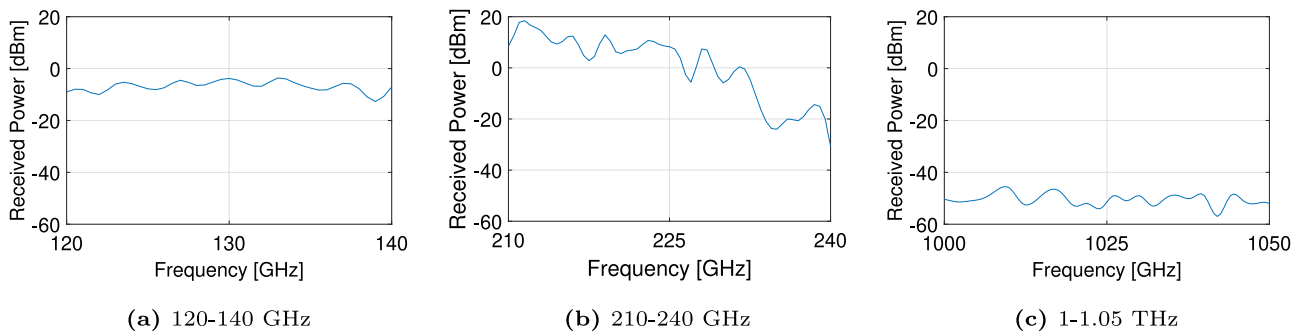


Fig. 4. Received power of the different front-ends within their bandwidth of operation.

$3.9 \times 10^{-17} \text{ W Hz}^{-1}$ for the 120–140 GHz, 210–240 GHz, and 1.00–1.05 THz receivers, respectively. It is relevant to note that the noise in the 210–240 GHz system is one order of magnitude larger than the other front-ends. This noise is in fact originated by the transmitter, in which the much larger transmission power achieved with the chosen frequency multiplying and mixing chain, which enables much longer communication links [23], results in higher noise too. Furthermore, another noise type affecting frequency-multiplied systems is phase noise, which is directly related to the chain of frequency multipliers utilized in the transceiver system. As we explain in detail in [24], we can compensate for the presence of phase noise by adjusting the maximum frame size.

Finally, as also illustrated in Fig. 2, we have multiple sets of broadband antennas with directivity gains ranging from 25 dBi up to 40 dBi at the aforementioned frequencies.

3. Offline 32-GHz signal processing back-end

In order to make the most out of the very large bandwidth available at THz frequencies, an ultra-broadband digital processing engine is needed. The first solution developed by our team is an offline digital back-end system based on an arbitrary waveform generator (AWG) at the transmitter and a digital storage oscilloscope (DSO) at the receiver, which can process signals with up to 32 GHz of baseband bandwidth per channel. A software-defined physical layer is utilized to define and generate the baseband/IF signals at the transmitter and, correspondingly, collect and process them at the receiver. MATLAB is chosen as the environment to develop the different signal processing blocks, as it ensures a rapid transition from theoretical and numerical analysis to experimental testing.

In [24], we provide a detailed description of this back-end. Here, we summarize its implementation and main features, and provide additional experimental results.

3.1. System overview and specifications

The fundamental building blocks of this system are the following. At the transmitter, a Keysight AWG M8196 A with a baseband bandwidth of 32 GHz and a sampling rate of up to 93.4 Giga-Samples-per-second (GSps) with 8-bit resolution is utilized to generate the signals to be up-converted. To define the samples at the input of the AWG, a software-defined physical layer is utilized to generate bits, encapsulate them within frames, and modulate the resulting binary sequence into symbols. Initially, to generate the frame, three parts are appended, namely, header, training sequence, and data sequence. The header is generally a sequence that provides optimal correlation properties, namely, high auto-correlation and low cross-correlation. The bits within the training sequence are utilized to estimate and equalize the channel. The generated frames are modulated and pulse shaped according to different single-carrier or multi-carrier modulation

Table 1
System specifications.

Parameter	Center frequency: 130 GHz	Center frequency: 220 GHz
Output Power	13 dBm	23 dBm
Tx/Rx antenna Gain	38 dBi	40 dBi
Receiver Mixer loss	7 dB	15 dB
Cable and connector loss	5.4 dB	5.4 dB
LNA gain	12 dB	35 dB

schemes. Finally, to compensate for the frequency-selective response of the hardware, a pre-equalization filter is utilized.

Reciprocally, at the receiver, a Keysight DSO Z632 A with a baseband bandwidth of 63 GHz and a sampling rate of up to 160 GSps with 8-bit resolution is utilized to capture, digitize, and store the received down-converted signals for further processing. As the first element of the software-defined physical layer, a bandpass filter with a high roll-off rate is utilized to restrict the out of band noise. To detect the starting point of the captured signal, the frame synchronization is performed by correlation with the known header sequence. After that, a post-equalization filter is utilized to mitigate the effect of the frequency selective nature of the channel. A correlation-type detector based on maximum likelihood (ML) criterion is utilized to detect the received signal. The structure of the general software-defined physical layer described here is summarized in Fig. 5.

3.2. Experimental results

We have utilized the back-end in conjunction with the three different front-ends to obtain different results in terms of propagation measurement, channel modeling, noise characterization, and data communication. In [24,25], we utilized this digital back-end to both characterize the 1.00–1.05 THz channel as well as to demonstrate multi-Gbps data transmission at *true* THz frequencies for the first time. More specifically, we measured the ultra-broadband THz channel in the case of line-of-sight (LoS) propagation and characterized the amplitude noise and the phase noise of the end-to-end system. Furthermore, the bit error rate (BER) of different data communication schemes, including M-PSK, M-PAM, chirp-based modulation, and OFDM modulation, were experimentally tested and analyzed. However, due to low transmit power (-15 dBm), the link distance with these front-ends is limited to tens of centimeters. While this is not enough for WiFi and cellular-type applications, this is meaningful in the case of short-range ultra-broadband links, such as Tbps wireless personal area networks and in multimedia kiosks [1].

When utilizing the lower frequency front-ends, the much larger transmission power enables many additional studies. Among others, the 120–140 GHz front-ends are utilized to characterize multi-path propagation in indoor and outdoor scenarios. In fact, the D-band (110–170 GHz) is currently receiving much attention by several groups worldwide [26,27], as the first practical window above 100 GHz. As

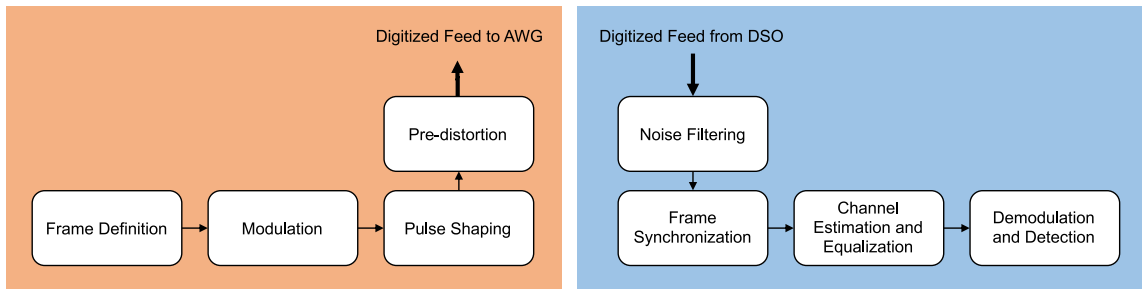


Fig. 5. Block diagram of the physical layer model implemented with the offline digital back-ends.

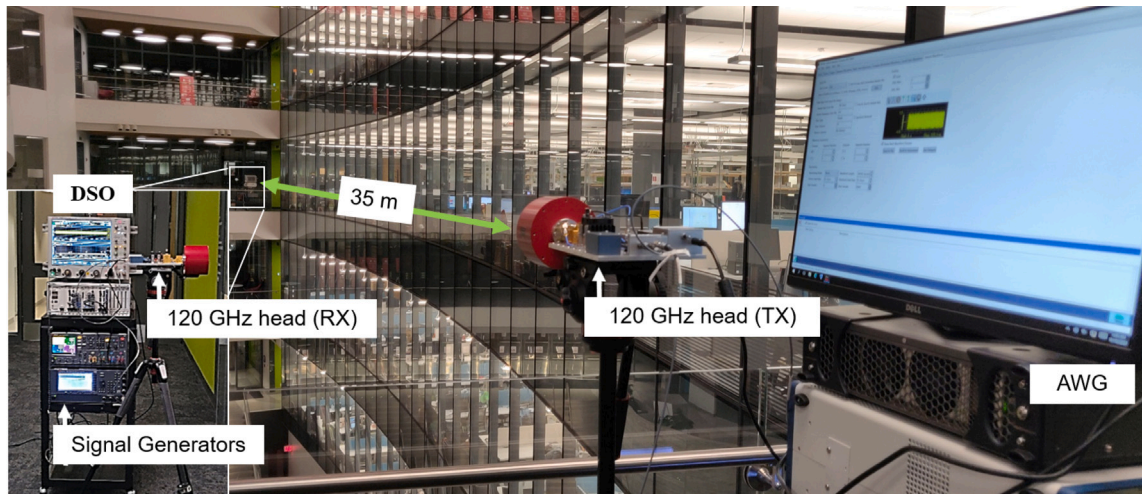
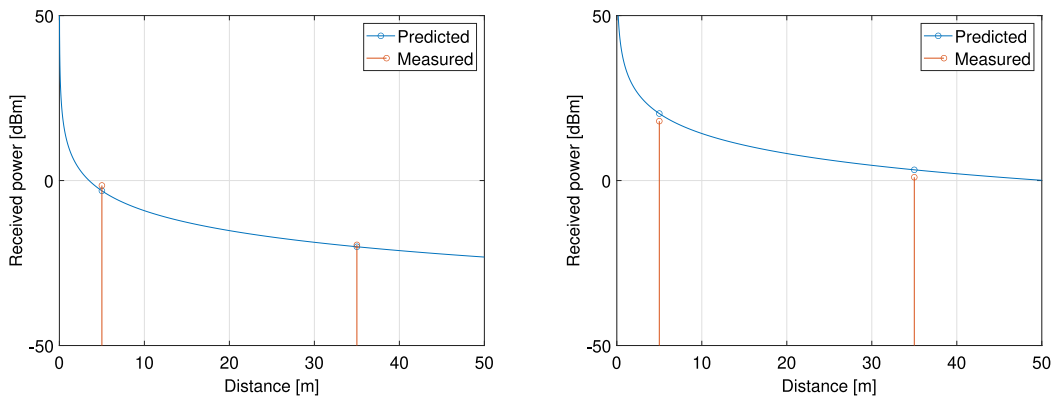


Fig. 6. Experimental setup of 35 m link with offline 32-GHz signal processing back-ends.



(a) Actual received power vs the predicted received power for 210-240 GHz based system. (b) Actual received power vs the predicted received power for 120-140 GHz based system.

Fig. 7. Link budget analysis based on a) 210–240 GHz front-ends and b) 120–140 GHz front-ends.

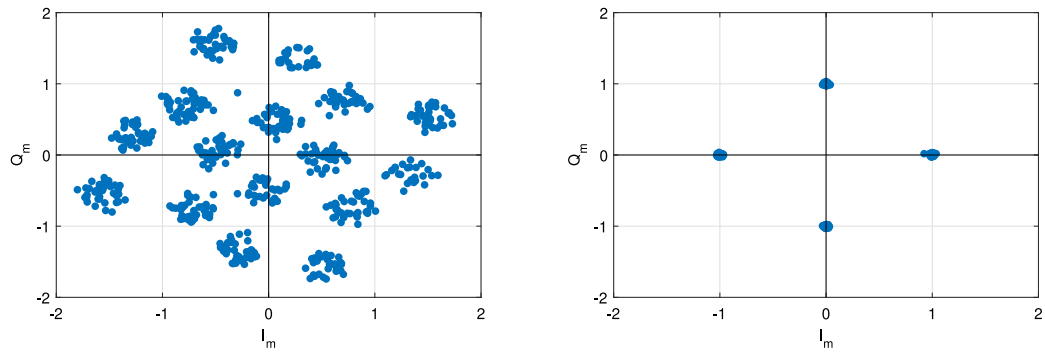
a preliminary result, the link budget analysis up to 35 m at 130 GHz of center frequency accounting for different components' specification, listed in Table 1, is demonstrated in Fig. 7(a). In particular, the received signal power P_{rx} in dB is given by,

$$P_{rx} = P_{tx} + G_{tx} + G_{rx} + G_{LNA} - L_{spread} - L_{abs} - L_{mixer} - L_{misc}, \quad (1)$$

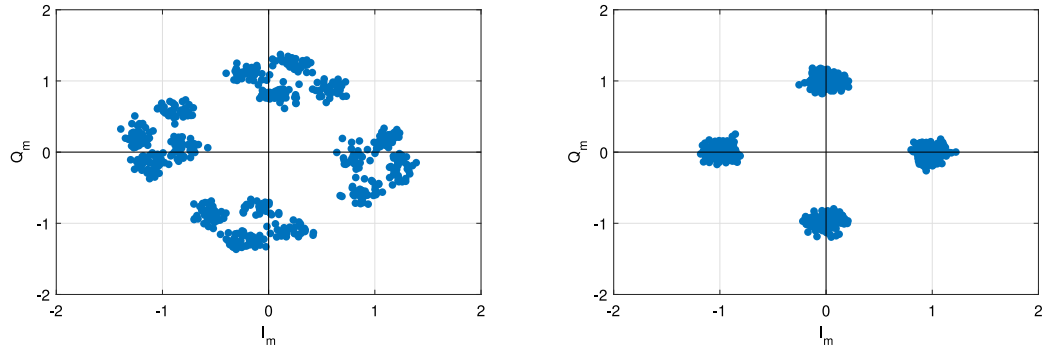
where P_{tx} is the transmitted signal power, G_{tx} and G_{rx} are the transmit and receive antenna gains, respectively, G_{LNA} refers to the gain of the LNA at the receiver, L_{spread} denotes the loss due to spreading, L_{abs} stands for the absorption loss, L_{mixer} is the conversion loss at receiver and L_{misc} accounts for miscellaneous losses in cables and connectors. Also, to exhibit the link performance, the BERs (obtained by averaging

over 10 frames with 1,200 bits each) for QPSK, 8-PSK, and 16-PSK schemes are demonstrated with the symbol rates 1 GSps and 2 GSps for 35 m and up to 10 GSps for 5 m in Table 2a. The experimental setup for 35 m is shown in Fig. 6, and a similar setup is utilized for the 5 m link shown in Fig. 9. Besides, error vector magnitude (EVM) values for different modulation schemes with different data rates are shown for a fair comparison. Furthermore, the constellation plot for the QPSK scheme is shown in Fig. 8(a) and (b) before and after equalization, respectively. The constellation diagram before the equalization block depicts the multi-path nature of the channel.

We have performed a similar study with the 210–240 GHz front-ends. The link budget analysis up to 35 m at 220 GHz of center



(a) Before post-equalization for 120-140 GHz based system. (b) After post-equalization for 120-140 GHz based system.



(c) Before post-equalization for 210-240 GHz based system. (d) After post-equalization for 210-240 GHz based system.

Fig. 8. Constellation diagram or QPSK obtained before and after equalization for 1 Gbps signal.

Table 2
BER for different modulation schemes.

(a) 120–140 GHz front-ends based system					
Modulation	Distance(m)	BW (GHz)/Data rate (Gbps)	SNR (dB)	BER	EVM (dB)
QPSK	5	10/10	31	0 ^a	-15.5
8-PSK	5	10/15	31	0 ^a	-15.3
16-PSK	5	10/20	31	8 × 10 ⁻⁵	-14.1
QPSK	5	15/15	27.2	0 ^a	-13.27
8-PSK	5	15/22.5	27.2	0 ^a	-13
16-PSK	5	15/30	27.2	8 × 10 ⁻⁵	-12.2
QPSK	5	20/20	26	0 ^a	-11
8-PSK	5	20/30	26	0 ^a	-10.9
16-PSK	5	20/40	26	1.6 × 10 ⁻⁴	-10.5
QPSK	35	2/2	23.5	0 ^a	-17.95
8-PSK	35	2/3	23.5	0 ^a	-17.5
16-PSK	35	2/4	23.5	0 ^a	-17.95
QPSK	35	4/4	21.1	0 ^a	-16.38
8-PSK	35	4/6	21.1	0 ^a	-16.5
16-PSK	35	4/8	21.1	8 × 10 ⁻⁵	-16
(b) 210–240 GHz front-ends based system					
Modulation	Distance(m)	BW (GHz)/Data rate (Gbps)	SNR (dB)	BER	EVM (dB)
QPSK	5	4/4	17.2	0 ^a	-9.5
8-PSK	5	4/6	17.2	0 ^a	-9.5
16-PSK	5	4/8	17.2	8 × 10 ⁻⁵	-9.3
QPSK	5	6/6	12.1	0 ^a	-5.08
8-PSK	5	6/9	12.1	2.5 × 10 ⁻³	-5.1
16-PSK	5	6/12	12.1	1.0 × 10 ⁻²	-5.1
QPSK	5	10/10	8.9	2.0 × 10 ⁻²	-3
8-PSK	5	10/15	8.9	1.4 × 10 ⁻¹	-3.1
16-PSK	5	10/20	8.9	1.8 × 10 ⁻¹	-3.3
QPSK	35	2/2	5.5	0 ^a	-10.45
8-PSK	35	2/3	5.5	0 ^a	-10.2
16-PSK	35	2/4	5.5	1.6 × 10 ⁻³	-10.2
QPSK	35	4/4	2.1	0 ^a	-7.6
8-PSK	35	4/6	2.1	8 × 10 ⁻⁵	-7.5
16-PSK	35	4/8	2.1	3 × 10 ⁻²	-7.2

^a0 BER: no bit error within 10 frames with 1,200 bits each.

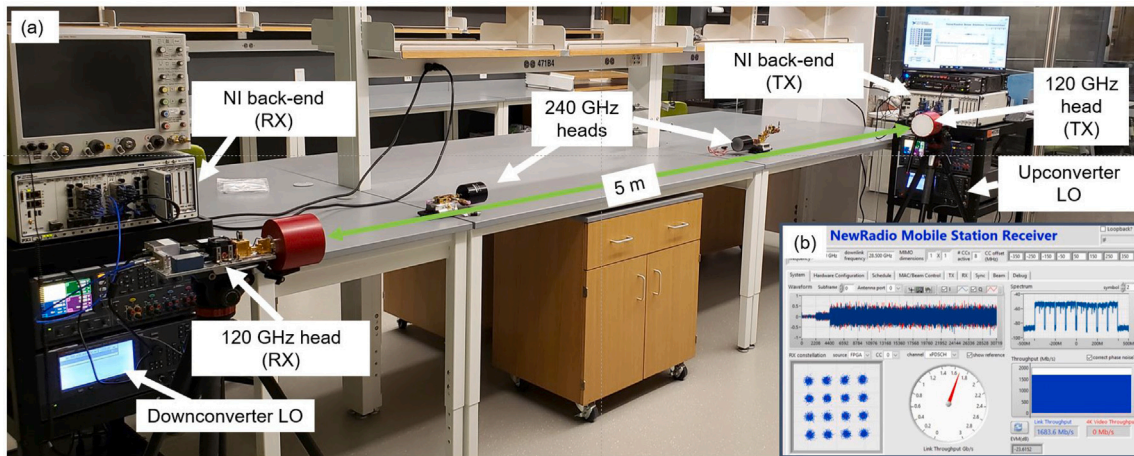


Fig. 9. (a) Experimental setup of the 5 m point-to-point link using the NI back-end and the 120–140 GHz and 220–240 GHz front-ends; (b) capture of NI receiver graphical front-end showing successful transmission using 16-QAM, 3/4 MCS.

frequency is illustrated in Fig. 7(b), and specifications of different components are listed in Table 1. Furthermore, the BERs for QPSK, 8-PSK, and 16-PSK schemes are demonstrated with the symbol rates up to 5 Gsps considering a communication link of 5 m distance. Performances of similar modulation schemes up to 2 Gsps symbol rates are also shown to demonstrate a longer communication link of 35 m (Table 2b). In parallel, the achievable EVM for different modulation with data rates are presented. Moreover, a constellation of QPSK without and with equalization (Fig. 8(c) and (d)) is shown side by side to portray a multi-path scenario and equalizer performance, respectively. Also, by utilizing higher gain antennas, much longer links are possible [23].

The experimental results presented in Table 2a and b show the expected increment in BER for higher order modulations and increased symbol rates. Similarly, a significant change in EVM is observed due to the change in distance and symbol rate. The effective SNR is reduced with an increase in link distance, which raises the EVM. Furthermore, the same sampling rate is utilized to capture the received signal (160 Gsps of DSO), which provides a higher over-sampling gain to the low symbol rate signal compared to the high symbol rate signal. Therefore, the signal with a lower symbol rate due to the lower noise floor and higher over-sampling gain has low EVM. However, due to higher phase noise and higher thermal noise floor of the 210–240 GHz front-ends compared to the 120–140 GHz front-ends, the EVM is higher for 210–240 GHz based system.

4. National-instruments-based 2-GHz signal processing back-end

The NI mmWave SDR platform [28] is a real-time transceiver system that implements the full PHY layer. The system enables real-time over-the-air (OTA) end-to-end experiments of wireless networks starting from physical layer to higher layers. The platform is built as an integration of different modules that involves baseband processing, data-converters, IF generation, and others, inside a NI PXIe-1085 Express chassis. Albeit the bandwidth of this platform is lower than that of the AWG/DSO setup, the NI platform allows the testing of new techniques in dynamical real-time conditions.

4.1. System overview and specifications

The NI platform integrates multiple high-performance FPGAs to handle the transmitter and receiver operations including modulation/demodulation in real-time. The IQ baseband interfaces can be accessed directly or can be connected through the upconverter/downconverter modules for IF operation. Apart from the TX/RX chain hardware, the chassis come with a high-end back-plane that

connects to a host machine. The host can be used for dynamic reconfiguration of modulation and coding schemes (MCSs), uplink/downlink slots and other control functions. The host can also be used to transfer data from the FPGA to the host (or vice-versa) through the high-speed backplane for generating source bits for transmission and for other debugging purposes.

The NI hardware supports two PHY layer implementations, namely, (i) a single-carrier (SC) baseband that resembles an LTE-A system, and (ii) an OFDM multi-carrier system, both supporting bi-directional transmission. The SC implementations supports 1.76 GHz of bandwidth whereas the OFDM supports 800 MHz. Detailed description of the SC system can be found in [29]. Both PHY implementations generally support multiple MCS combinations, including 1/5 BPSK, 1/4 QPSK, 1/2 QPSK, 3/4 QPSK, 1/2 16-QAM, 3/4 16-QAM, 7/8 16-QAM, 3/4 64-QAM, and 7/8 64-QAM with a theoretical maximum bit rate of ≈ 4.8 Gbps and ≈ 3 Gbps for SC and OFDM, respectively.

4.2. Experimental results

The THz front-ends (Section 2) accept/generate an IF as the input/output of the transceiver system. Therefore, the NI back-ends can be used in IF mode to interface with the front-ends described in Section 2. The 1 THz front-end has limited transmit power (30 μ W max transmit power) and thus needs high sensitivity data converters at the receiver-end to recover the signals. The NI ADCs have a lower dynamic range with higher minimum sensitivity and therefore, currently only the 120–140 GHz heads and the 220–240 GHz heads can be used with NI back-ends.

We have used the NI nodes to demonstrate end-to-end wireless communication over 100 GHz using the capabilities of the testbed. The experiments were conducted by using the NI system in the IF-mode to generate the digital baseband and thereby interfacing the IF to the front-ends. Multiple experiments were performed at different distances over 120–140 GHz and 220–240 GHz frequency bands. The OFDM PHY was used for testing the point-to-point links at 5 m and 35 m distances. Fig. 9(a) shows the experimentation setup for the 5 m link (depicts an experiment conducted using the 120–140 GHz heads, same setup was used to repeat the experiments by changing to 220–240 GHz heads). The same set of experiments was conducted at 35 m distance using the setup shown in Fig. 6. The IF out center frequency was set to 10.65 GHz at the transmitter-side NI node. The transmit-side upconverter frequency was set to 130 GHz (LO output frequency from the oscillator was 130 GHz/4) for the experiment with 120–140 GHz heads, while the other transmission was conducted at 216 GHz (LO input frequency was 216 GHz/9). The receiver-side downconverter LO was offset by 1 GHz to avoid phase noise becoming an amplitude

Table 3

Throughput (Thrpt) results obtained by interfacing the NI digital back-end with the 120 GHz and 240 GHz front-ends using the OFDM PHY in a 5 m link (theoretical maximum throughput values calculated accounting one control slot in a subframe)

MCS	Thrpt (Mbps) at 5 m		Thrpt (Mbps) at 35 m		Theoretical Thrpt (Mbps)
	120 GHz	240 GHz	120 GHz	240 GHz	
BPSK 1/5	118	118	118	118	118
QPSK 1/4	272	272	272	248	297
QPSK 1/2	567	567	567	280	594
QPSK 3/4	824	824	824	125	891
16-QAM 1/2	1192	1192	800	No Thrpt	1188
16-QAM 3/4	1683	1677	652	No Thrpt	1782
16-QAM 7/8	1978	1091	348	No Thrpt	2080
64-QAM 3/4	2474	No Thrpt	No Thrpt	No Thrpt	2674
64-QAM 7/8	2890	No Thrpt	No Thrpt	No Thrpt	3120

modulation at the received signal by setting the first stage downconverter LO to 131 GHz. To account for the offset the second IF-stage oscillator frequency at the receiver-side NI node was set to 9.65 GHz. Table 3 tabulates the experimentally obtained throughput values for the wireless links established at the two frequencies using different MCSs for the two distances. The theoretical expected throughput values have also been shown for the comparison purpose. As seen from the table, the 220–240 GHz system achieves no throughput for the 64-QAM MCSs even for the short range link due to high noise floor of the front-ends which leads to poor SNR at the receiver.

5. Xilinx RFSoc based signal processing back-end

The fact that the NI real-time back-end engine only supports up to 1.76 GHz of bandwidth is a bottleneck to conduct real-time research in the THz frequencies, especially, for utilizing the enormous bandwidth opportunity available at these frequencies for real-time experimentation involving higher layers. Authors are also not aware of any other commercial (or non-commercial) software-defined-radio/digital back-end platform that can support bandwidths in excess of 2 GHz in real-time. Thus, there is a critical need of having real-time digital signal processing engine (DSP) engines able to process multi-GHz of bandwidth for advancing the research/experimentation at above 100 GHz frequencies which will unleash the full potential in the THz band. To this end, in this section we present a possible approach for addressing this concern. We envision a real-time multi-channel baseband able to independently manipulate and, when required, jointly aggregate multi-GHz-wide channels that can be up/down-converted by the aforementioned front-ends spanning across multiple THz frequency bands. Such an effort will enable real-time communication at these frequency bands which is a limitation of our current testbed.

We believe that a possible approach for realizing ultrabroadband signals with digital back-ends would be to use data links consisting of multiple frequency multiplexed radio channels which would allow digital processors to process slower manageable bandwidths. Using multiple ADC/DAC chips to interface sampled data to the processor through high-speed interfaces is infeasible due to prohibitive hardware complexity and power consumption. Therefore, we propose a back-end system where a system-on-a-chip (SoC) with multiple data converters (preferably supporting GSps rates) integrated on the same chip alongside the digital logic for reconfigurable SDR. Each low-bandwidth channel is processed on its own digital back-end leading to a multi-channel SDR processor. For this, we exploit the Xilinx radio-frequency SoCs (RFSoc) to enable low size-weight-and-power (SWaP) realization of frequency multiplexed multichannel SDRs. These SoC integrations eliminate the large number of external interfaces required for interfacing analog signals and thereby facilitate deployment of higher number of channels in a smaller foot print with greatly reduced power consumption. Thus, the system that is proposed (which is being implemented), will leverage the RFSoc chips [30] for implementing digital back-ends at both the transmitter and the receiver side.

5.1. System overview and specifications

The Xilinx RFSocS were released a few years back and the device's first generation supported up to 16 DACs and ADCs that can be clocked up to 6.55 GSps and 4.096 GSps respectively. Up to now these devices have been primarily used for realizing MIMO and phased array solutions for 5G mmWave applications to interface multi-antenna systems with digital back-end [31–34]. Instead, we propose to use the on-chip multiple DACs and ADCs available in the RFSocS to multiplex multiple low-bandwidth slower channels to process a multichannel high bandwidth signal to support real-time wireless links at tens to hundreds of Gbps. The overview architecture of the proposed real-time back-end processing system is shown in Fig. 10.

The current implementation uses the ZCU111 RFSoc evaluation boards which feature the 1st generation Xilinx ZU29DR RFSoc chips. This particular chip supports 8 DACs and 8 ADCs which can be clocked at a max rate of 6.55 GSps and 4.096 GSps, respectively. Thus, ideally supporting $2.048 \text{ GHz} \times 8 = 16.4 \text{ GHz}$ of total bandwidth at the ADCs and $3.27 \text{ GHz} \times 8 = 26.2 \text{ GHz}$ at the DACs. Each DAC has a 14-bit resolution whereas the ADCs come with 12-bit precision. The programmable logic (PL) part or the FPGA fabric of the chip comprises of 930K logic cells and over 4K DSP slices, along with 60.5 Mb of block RAM memory. The RFSoc also has four ARM Cortex-A53 cores and two ARM Cortex-R5 cores hardened which can be used to run real-time OSS, or bare metal application for real-time communication/processing with PL. The ZU29DR RFSoc chip also come with eight hardened soft-decision forward error correction (SD-FECs) IP blocks [30]. These IPs support LDPC encoding/decoding and Turbo decoding. Such integrations enable low latency, multi-Gbps data rates compared to soft cores and saves FPGA resources for other logic implementation. The ZCU111 platform in particular supports, 4 SFP+ optical connections to PL to support data high data rate in and out streaming. One Gbps Ethernet connectivity has been provided for APU side as high speed connectivity through APU.

For the full system design shown in Fig. 10, minimum of maximum clockable frequencies at both DACs and ADCS, which is 4.096 GSps will be used. To relax the analog filtering requirements of both anti-imaging and anti-aliasing filters, $2\times$ interpolation/decimation is used at DACs and ADCs, respectively. As shown in Fig. 10(a), 2 DACs (out of 8) are used to generate/process a single channel (complex baseband) of 2.048 GHz at the transmitter. Thus, in total 4 such baseband channels can be accommodated (given that $4\times$ the logic can fit in to the PL, which will be mostly critical at the receiver-side). The architecture of the receiver-side baseband processing back-end is similar to the transmitter-side and is shown in Fig. 10(b). Each downconverted baseband channel will be quadrature sampled using 2 ADCs at 4.096 GHz and will be decimated $2\times$ before processing.

It should be noted here that, although we use Gen-1 ZCU111 RFSoc board in our current implementation, if a testbed contains multiple ZCU111 boards, these cannot be synchronized easily—a problem for SDRs having bandwidths greater than 16 GHz that would need some sort of synchronization among the channels. The ZCU111 has been

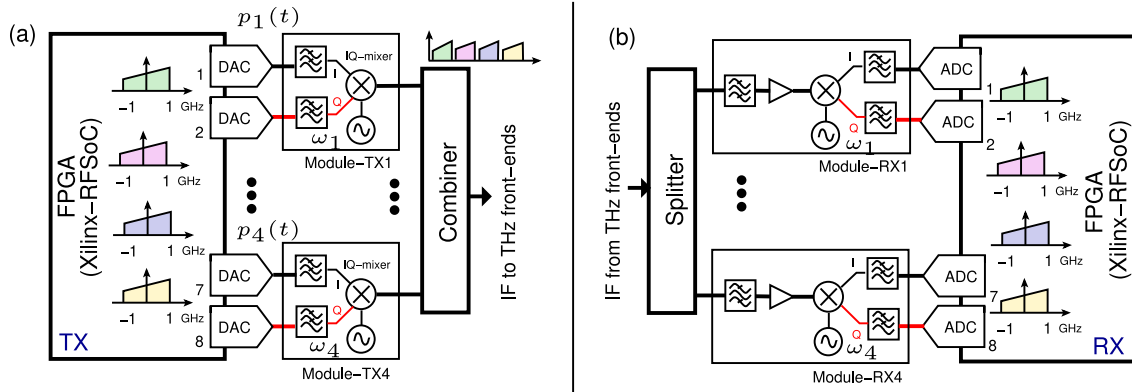


Fig. 10. Overview architecture of the RFSoc based real-time back-end; (a) transmitter side, (b) receiver-side.

replaced by Gen-3 Silicon, leading to ZCU-208 board. This latest board supports 8 ADC/DACs, with ADCs operating up to 5 GSps, and DACs operating up to 10 GSps, and multiple ZCU-208 boards can be locked to a reference clock when such synchronization is necessary in the underlying signal processing operation (e.g., beamformers, correlators). Furthermore, Xilinx provides a variety of 16x16 ADC/DAC RF-SoC boards, such as ZCU-1275, ZCU-1285, and ZCU-216. These boards are less practical because the relatively small bandwidths supported on a per channel basis at the ADC-side. Ultimately, we are providing a vision and path moving forward, not necessarily tied to a specific RFSoc generation.

Analog RF Circuits. At the transmitter, each baseband channel has to be properly frequency multiplexed to form an aggregated fat IF output to be fed in to the THz front-ends. This will be achieved through a set of IQ-mixers, that will upconvert the baseband channels to different IF carriers ω_k , $k \in \{1, 2, 3, 4\}$, where $2 \text{ GHz} < \omega_k < 18 \text{ GHz}$. The ω_k frequencies will be carefully chosen to allow a sufficient guard between the channels and avoid inter-channel harmonic distortions. The upconverted frequency multiplexed channels will ultimately be combined using a wideband combiner to form an aggregated IF that will be sent to THz front-ends.

The receiver-side will be designed in a similar fashion to undo the aggregated channels in the received IF. To achieve this, the received IF will be split into 4. Then each output will be subjected to a bandpass filtering at each ω_k center frequency to filter out each 2 GHz wide channel. A set of amplifiers will be used to maintain the required cascaded gain in each channel. The separated IF signals centered at different ω_k frequencies then will be direct converted back to baseband using a set of IQ mixers with local oscillators tuned to ω_k . The downconverted IQ channels will be lowpass filtered and sampled separately in to the RFSoc.

Digital Baseband Processing. Although the data converters of the RFSocs can be clocked at speeds exceeding 4 GHz, the maximum rate the PL fabric can be clocked is about an order of magnitude less than the maximum sampling rates. Thus, efficient polyphase digital circuit architectures are required for processing such high bandwidth signals. Therefore, digital circuits are designed in a polyphase manner for PHY processing while leveraging the maximum bandwidth supported by data converters.

PHY Layer Specifications. For the initial implementation, the PHY layer is chosen to be based on OFDM. Due to the ultra-wide bandwidth supported by the front-ends of the current testbeds, a stronger contribution to the overall channel frequency selectivity comes from the hardware electronics. Initial measurements using the 120 GHz front-ends (discussed in Section 2.1) were carried out to determine the sub-carrier spacing such that the subchannels can be regarded frequency flat. The measurement showed that this is met for bandwidths $< 50 \text{ MHz}$ per subcarrier and thus an FFT size of 64 was used to design the PHY layer. Since the baseband (including the OFDM processor)

is clocked at 2.048 GHz, subcarrier spacing for the implementation is 32 MHz. The digital cores are designed to support up to 64-QAM modulations with the option of adaptive modulations at subcarrier-level. PHY layer frame structure has been implemented with close resemblance to 802.11a standard due to the choice of 64-point FFT size.

5.2. Prototype system and preliminary experimental results

A prototype system having the architecture discussed above is currently being developed. To start with, the transmitter side has been implemented using the Xilinx ZCU111 board. The DACs are driven at 4.096 GSps with $2\times$ upsampling with FPGA circuits running effectively at 2.048 GSps. A 16-phase polyphase digital architecture is used to implement the PHY processing. For demonstration purpose, two baseband channels were generated from the RFSoc and two IQ mixers with LOs operating at $\omega_1 = 3 \text{ GHz}$ and $\omega_2 = 5.5 \text{ GHz}$ were used to up convert the signals. The two 2 GHz channels were then aggregated to form a 4 GHz IF using a 2-way combiner.

Fig. 11(a) shows the transmitter platform that has been built. Fig. 11(b) shows the frequency domain plot of the combiner IF output having 4 GHz of aggregated bandwidth where each channel having 2 GHz of bandwidth are combined (channel-1 centered at 3 GHz carrying BPSK modulated data and channel-2 centered at 5.5 GHz with QPSK modulated data). The scope-captured wave-forms at IF have been software-processed for validating the proper operation of the transmit-side digital circuits and the recovered constellations corresponding to the two channels have been shown in Fig. 12. The calculated EVM values were -19.5 dB and -17.2 dB for the channel 1 and 2, respectively.

System is currently being extended to 4 channels to support 8 GHz of bandwidth at the transmitter side leveraging all 8 DACs of the ZU28DR chip. RFSoc based receiver-side processing node is also being developed along with the multi-channel demultiplexing front-end to bring the IF channels to baseband.

6. Conclusion

Currently, the experimental research in THz communications has been limited to characterizing the THz channel and demonstrating new THz devices that are focused on implementing the traditional communication techniques. To push the THz research forward, non-traditional communication and networking solutions tailored to the capabilities of THz devices and the peculiarities of the THz channel that can be found in the related literature need to be experimentally tested and refined. A versatile experimental platform that consists of different front-ends covering important absorption defined windows in the THz band and different signal processing back-ends that can be used depending on the experimentation requirements has been presented in this paper. The paper also details experimental results of wireless links obtained at multiple carrier frequencies in the THz band using the different capabilities of the signal processing back-ends available as a part of the testbed.

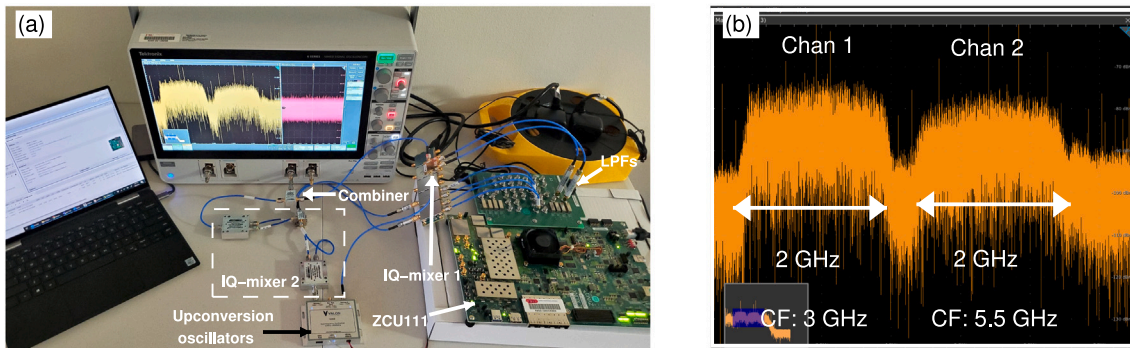


Fig. 11. (a) Experimental prototype of the proposed transmitter-side back-end. (b) Scope capture of the output at the combiner which aggregates 4 GHz of bandwidth by multiplexing two 2 GHz channels (centered at 3 and 5.5 GHz); Xilinx ZCU111 board is used to generate the 2 GHz channels using 4 of the DACs out of 8 (CF denotes the center frequency).

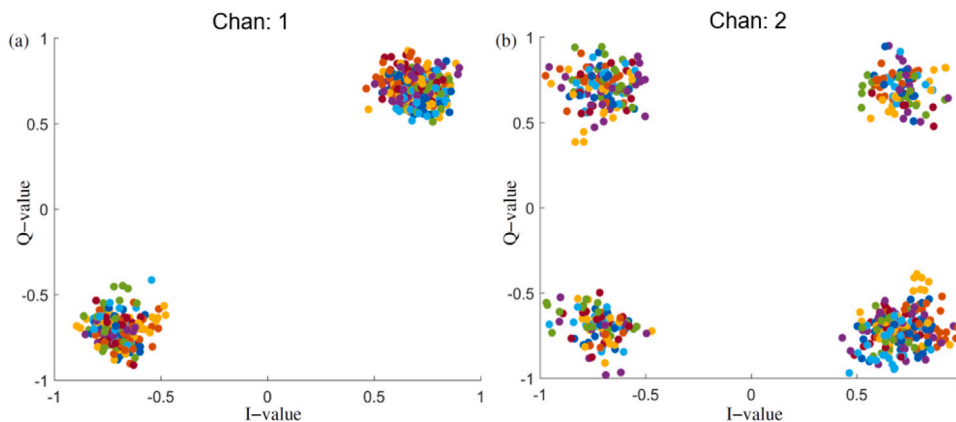


Fig. 12. Software processed constellation diagrams corresponding to the two-channels at IF.

CRedit authorship contribution statement

Priyanshu Sen: Conceptualization, Methodology, Writing - original draft, Writing - review & editing. **Viduneth Ariyaratna:** Conceptualization, Methodology, Writing - original draft, Writing - review & editing. **Arjuna Madanayake:** Conceptualization, Supervision, Validation. **Josep M. Jornet:** Conceptualization, Supervision, Funding acquisition, Validation.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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