Experimental Wireless Testbed for Ultrabroadband Terahertz Networks

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Abstract

Communication at terahertz (THz) frequencies will be a key component of the 6th generation (6G) wireless networks and beyond. In this paper, a state-of-the-art wireless platform that supports three major frequency bands above 100 GHz in the THz band is presented. The specifications of the overall THz experimental platform built by Northeastern University are discussed, detailing the capabilities of the different available THz front-ends and signal processing back-ends. Moreover, an ongoing effort to build a scalable real-time back-end engine that supports multiple multi-GHz-wide channels at baseband is also presented. Preliminary results of the transmitter-side implementation are presented with a detailed overview of the envisioned system.

CCS Concepts: • **Networks → Wireless access networks**; • **General and reference → Experimentation**.

Keywords: terahertz communications, ultra-broadband networks, 6G, experimental research

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1 Introduction

The advent of millimeter wave (mmWave) fifth generation (5G) wireless systems has solved the spectrum scarcity problem in the sub-6 GHz bands to a great extent [20]. The commercial 5G mobile networks that are presently being rolled out in the 24-39 GHz bands and the wireless local area networks (WLAN) in the 60 GHz band come with a promise to deliver user data rates of up to 20 and 100 Gigabits-per-second (Gbps), respectively. However, the continuous proliferation of wireless technologies for communications, augmented reality, cloud robotics, smart health care, wireless internet of things (IoT) and radio-frequency (RF) sensing, among others, has resulted in increased demands for faster throughput and higher network capacity. Thus, wireless networks that can support data rates of up to 1 Terabit-per-second (Tbps) will become a reality soon. The only way seen to achieve such data rates is to move to carrier frequencies above 100 GHz [19] making use of the swath of uncharted bandwidth available at THz frequencies (100 GHz-10 THz). Although, moving directly to optical frequencies (infrared, visible or even ultra-violet, 100-750 THz) can be an option, the THz band is the first stop, which already possesses a very large bandwidth and has advantageous propagation characteristics when compared to optical frequency bands.

Notable initiatives can be seen worldwide for regulating the above 100 GHz spectrum towards 6G research activities. The new Federal Communications Commission (FCC) policy in the US has created a new category of experimental licenses for use of frequencies between 95 GHz and 3 THz and makes a total of 21.2 GHz of spectrum available for use by unlicensed devices [30]. In particular, multiple bands in the 110–160 GHz and 200–260 GHz have been allocated to fixed/mobile usage (e.g., 122.25–123, 134–136, 231–235, 238–241 GHz). These bands become available with promise of coexistence with active and passive incumbents (mainly due to the very high sensitivity of the measurement equipment on board of Earth and space exploration satellites, as per the US246/5.340 footnotes in the FCC Table of Frequency Allocations [30]). Thus, aforementioned frequency bands have drawn much attention for experimentation exploiting the high bandwidth on offer especially for applications like wireless back-haul links.

Significant progress has occurred for THz communications due to recent advancements in electronic and photonic devices [25], accompanied by the technological demonstrations [11, 21]. Considerable work has been carried out for theoretical modelling of the THz channel [7, 27] and a handful of experimental measurements of the THz channels have also been reported, mainly at 100 GHz [32] and 300 GHz [4].

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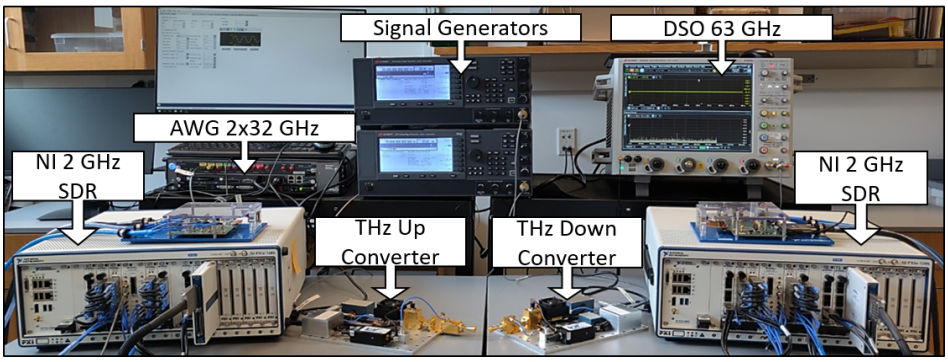


Figure 1. Ultrabroadband networking systems testbed at Northeastern University.

Physical layer (PHY) solutions that leverage the behavior of the THz channel have also been developed [12, 14], but very little [8] experimental validation being reported. Furthermore, first thoughts on higher layers can be found in [6, 31], but hitherto, no THz network-level demonstration has ever taken place. While network simulation tools exist [9], these are only the first step.

In order to advance THz communication research, there is tremendous interest in developing software defined radio (SDR) hardware and architectures that not only support THz frequencies, but also process digital basebands with tens to hundreds of GHz of bandwidth, targeting emerging 6G networks. In this paper, we detail the recent state-of-the-art platforms developed at Northeastern University (Figure 1) as well as a long-term vision of what is required for filling the need. The current testbed provides a versatile platform that covers three key THz frequency bands supporting different bandwidths while being able to perform different functionalities, starting from channel modeling to physical and networking layer implementation in real-time. For the purpose, various signal processing units are utilized at the back-end to support the required functionality.

In the following sections, we elaborate on the different aspects of the testbed starting from the available different THz front-ends providing their working principles and specifications (Section 2). Next, we walk through the back-end processing capabilities, detailing the offline 32 GHz ultrabroadband processing engine that offers the highest flexibility (Section 3). Afterwards, the 2 GHz National Instrument (NI) software defined radio platform (Section 4) is presented that adds the real-time experimentation capabilities to the testbed. Finally, we describe our ongoing work on building a customized real-time multi-GHz multi-channel digital signal processing engine where we propose the use of Xilinx radio frequency system-on-chip (RFSoC) based digital back-ends with processing bandwidths greater than 2 GHz (Section 5).

2 Terahertz (THz) Front-ends

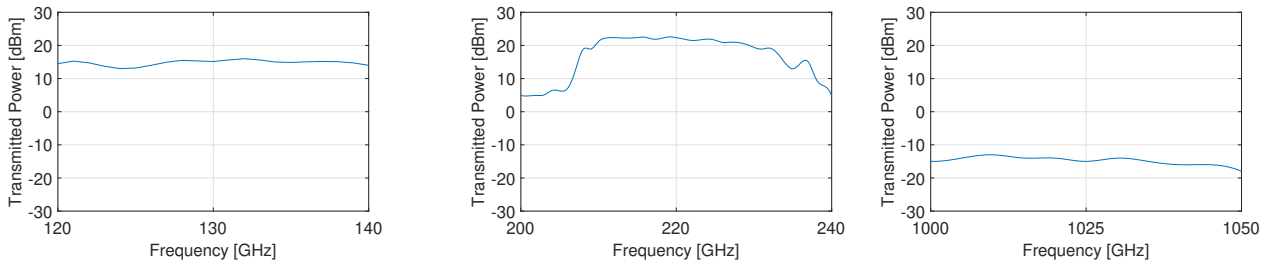
The key capability of a THz communication testbed is its ability to generate, modulate, radiate, detect and demodulate signals at THz frequencies. In our platform, we have three different sets of THz front-ends able to operate between 120-140 GHz, 200-240 GHz and 1.00-1.05 THz, respectively. Despite the different operation frequency, the three sets are based on the same architecture and technology, namely, frequency multiplying, amplifying and mixing chains based on Schottky diode technology [3]. In all the setups, the starting point is also always the same, i.e., a stable multi-GHz sinusoidal signal or local oscillator (LO), in our case provided by identical but separate analog signal generator (Keysight E8257D) at the transmitter and the receiver. Next, we describe the specifications of each front-end.

2.1 120-140 GHz Front-ends

The 120-140 GHz front-ends are custom-designed by Virginia Diodes Inc. (VDI). The transmitter consists of two frequency doublers, i.e., a total multiplication factor of ×4, to generate the carrier signal starting from a LO signal of 30-35 GHz. Thereafter, a mixer with 7 dB of double sideband conversion loss is utilized to modulate the carrier signal with the information-bearing broadband baseband/IF signal. At RF, a maximum output power of 13 dBm or 20 mw is achieved by an RF power amplifier with 20 dB gain. To down-convert the RF signal to baseband/IF, an identical setup is utilized to generate a THz carrier signal at the receiver side, which is mixed with the received RF signal. The down-converter with a low noise mixer is utilized to obtain the IF signal. For further amplification of the received signal, a low noise amplifier (LNA) with 12 dB gain is used at the IF stage, given the lack of LNA at RF.

2.2 200-240 GHz Front-ends

The front-ends at 200-240 GHz have been developed in collaboration with the NASA Jet Propulsion Laboratory (JPL) and leverage NASA's patented multiplier technology based on on-chip power combining [16, 26]. The measured output power is a world-record-setting 23 dBm (200 mW) at the given frequency range. The up-converter is based on a ×9 multiplier chain and is used to generate the RF signal from the LO signal of 22.2-26.67 GHz. A high power mixer with 7 dB of conversion loss is utilized to modulate the carrier



(a) 120-140 GHz **(b)** 200-240 GHz **(c)** 1-1.05 THz

Figure 2. Maximum transmitted power of the different front-ends within their bandwidth of operation.

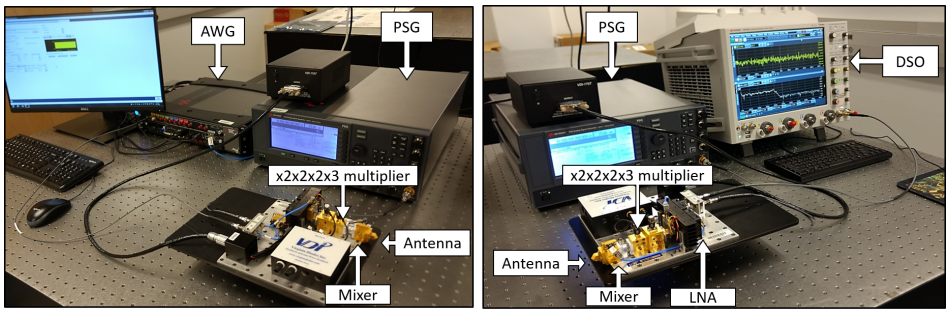


Figure 3. The offline digital back-end with the 1.00-1.05 THz front-ends.

with the information-bearing signal. The receiver's down-converter is based on a ×6 frequency multiplier-amplifier chain, and with the aid of a mixer, the RF signal is shifted down to the IF range. An IF stage LNA with 35 dB of gain is utilized to provide the required amplification.

2.3 1.00-1.05 THz Front-ends

Similar to the 120-140 GHz system, the 1.00-1.05 THz front-ends are custom designed by VDI. However, these possess a higher-order multiplier chain of ×24 (×2×2×2×3), which is utilized to generate the carrier from the LO signal ranging between 41.67-43.75 GHz. A sub-harmonic frequency mixer with 15 dB of conversion loss is utilized to modulate the carrier according to the IF signal. The maximum output power of the transmitter front-end is -15 dBm or 30 μw. At the receiver, an equivalent multiplier chain and low noise mixer with 15 dB of conversion loss are employed to obtain the IF signal from the received RF signal. Furthermore, an IF stage LNA with 10 dB of gain is used.

In Figure 2, we exhibit the maximum transmitted power for the three front-ends within their operational bandwidth to highlight the ultra-broadband nature of the testbed. We have sets of broadband antennas with directivity gains ranging from 25 dBi up to 55 dBi at the aforementioned frequencies.

3 Offline 32-GHz Signal Processing Back-End

In order to make the most out of the very large bandwidth available at THz frequencies, an ultra-broadband digital processing engine is needed. The first solution developed by our team is an offline digital back-end system based on an arbitrary waveform generator (AWG) at the transmitter and a digital storage oscilloscope (DSO) at the receiver, which can process signals with up to 32 GHz of baseband bandwidth per channel. A software-defined physical layer is utilized to define and generate the baseband/IF signals at the transmitter and, correspondingly, collect and process them at the receiver. MATLAB is chosen as the environment to develop the different signal processing blocks, as it ensures a rapid transition from theoretical and numerical analysis to experimental testing. As an example, the system is shown with the 1.00-1.05 THz front-ends in Figure 3. Next, we summarize the key specifications and provide a sub-set of the experimental results obtained with this digital back-end. All the details of the platform and experimental results with the 1.00-1.05 THz front-ends can be found in [24].

3.1 System Overview and Specifications

The fundamental building blocks of this system are the following. At the transmitter, a Keysight AWG M8196A with a baseband bandwidth of 32 GHz and a sampling rate of up to 93.4 Giga-Samples-per-second (GSps) with 8-bit resolution is utilized to generate the signals to be up-converted. To define the samples at the input of the AWG, a software-defined physical layer is utilized to generate bits, encapsulate them within frames, and modulate the resulting binary sequence into symbols. Initially, to generate the frame, three parts are appended, namely, header, training sequence, and data sequence. The header is generally a sequence that provides optimal correlation properties, namely, high auto-correlation

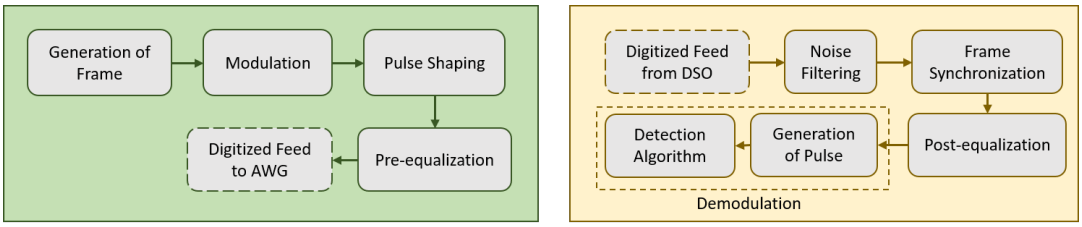


Figure 4. Block diagram of the physical layer model implemented with the offline digital back-end.

and low cross-correlation. The bits within the training sequence are utilized to estimate and equalize the channel. The generated frames are modulated and pulse shaped according to different single-carrier or multi-carrier modulation schemes. Finally, to compensate for the frequency-selective response of the hardware, a pre-equalization filter is utilized.

Reciprocally, at the receiver, a Keysight DSO Z632A with a baseband bandwidth of 63 GHz and a sampling rate of up to 160 GSps with 8-bit resolution is utilized to capture, digitize, and store the received down-converted signals for further processing. As the first element of the software-defined physical layer, a bandpass filter with a high roll-off rate is utilized to restrict the out of band noise. To detect the starting point of the captured signal, the frame synchronization is performed by correlation with the known header sequence. After that, a post-equalization filter is utilized to mitigate the effect of the frequency selective nature of the channel. A correlation-type detector based on maximum likelihood (ML) criterion is utilized to detect the received signal. The structure of the general software-defined physical layer here described is summarized in Figure 4.

3.2 Experimental Results

We have utilized this back-end in conjunction with the three different front-ends. In [23, 24], we utilized this digital back-end to both characterize the 1.00-1.05 THz channel as well as to demonstrate multi-Gbps data transmission at *true* THz frequencies for the first time. More specifically, we measured the ultra-broadband THz channel in the case of line-of-sight (LoS) propagation and characterized the amplitude noise and the phase noise of the end-to-end system. Furthermore, the bit error rate (BER) of different data communication schemes, including M-PSK, M-PAM, chirp-based modulation, and OFDM modulation, were experimentally tested and analyzed. However, due to low transmit power (-15 dBm), the link distance with these front-ends is limited to tens of centimeters. While this is not enough for WiFi and cellular-type applications, this is meaningful in the case of short-range ultra-broadband links, such as Tbps wireless personal area networks and in multimedia kiosks [1].

When utilizing the lower frequency front-ends, the much larger transmission power enables many additional studies. Among others, we are utilizing the 200-240 GHz front-ends to characterize multi-path propagation in indoor and outdoor scenarios. As a preliminary result, the link budget analysis up

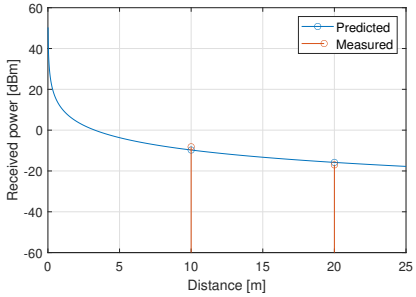
Table 1. Sample experiment specifications and performance.

System Specifications

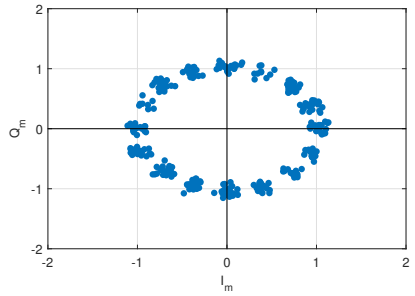
Parameter	Value
Center frequency	220 GHz
Output Power	23 dBm
Tx/Rx antenna Gain	25 dBi
Receiver Mixer loss	15 dB
Cable and connector loss	5.4 dB
LNA gain	35 dB

BER for different modulation schemes at 10 m

Modulation	Data rate (Gbps)	SNR (dB)	BER
16-PSK	4	35	0
32-PSK	5	35.6	1.9×10^{-2}
64-PSK	6	36	1.0×10^{-1}



(a) Actual received power vs the predicted received power.



(b) Constellation of a 16-PSK at 200-240 GHz over 10 m.

Figure 5. Experimental results obtained with 200-240 GHz front-ends by offline processing.

to 20 m at 220 GHz of center frequency accounting different components' specification, listed in Table 1, is demonstrated in Figure 5(a). Also, to demonstrate the link performance, BERs (obtained by averaging over 10 frames with 1,200 bits each) for 16-PSK, 32-PSK, and 64-PSK schemes with the similar symbol rate of 1 Gbps considering a communication

link of 10 m are illustrated in Table 1. Furthermore, the constellation plot for 16-PSK scheme is shown in Figure 5(b). By utilizing higher gain antennas, much longer links are possible [13].

Similar studies are being performed with the 120-140 GHz front-ends. In fact, the D-band (110-170 GHz) is currently receiving much attention by several groups worldwide [2, 17], as the first practical window above 100 GHz.

4 National-Instruments-based 2-GHz Signal Processing Back-End

4.1 System Overview and Specifications

The NI SDR platform [15] is a real-time transceiver system that implements the full PHY layer. The system enables real-time over-the-air (OTA) end-to-end experiments of wireless networks starting from physical layer to higher layers. The platform is built as an integration of different modules that involves baseband processing, data-converters, IF generation, and others, inside a NI PXIe-1085 Express chassis. Albeit the bandwidth of this platform is lower than that of the AWG/DSO setup, the NI platform allows the testing of new techniques in dynamical real-time conditions.

The NI platform integrates multiple high-performance FPGAs to handle the transmitter and receiver operations including modulation/demodulation in real-time. The IQ baseband interfaces can be accessed directly or can be connected through the upconverter/downconverter modules for IF operation. Apart from the TX/RX chain hardware, the chassis come with a high-end back-plane that connects to a host machine. The host can be used for dynamic reconfiguration of modulation and coding schemes (MCSs), uplink/downlink slots and other control functions. The host can also be used to transfer data from the FPGA to the host (or vice-versa) through the high-speed backplane for generating source bits for transmission and for other debugging purposes.

The NI hardware supports two PHY layer implementations, namely, (i) a single-carrier(SC) baseband that resembles that of an LTE-A system, and (ii) an OFDM multi-carrier system, both supporting bi-directional transmission. The SC implementations supports 1.76 GHz of bandwidth whereas the OFDM supports 800 MHz. Detailed description of the SC system can be found in [22]. Both PHY implementations generally support multiple MCS combinations, including 1/5 BPSK, 1/4 QPSK, 1/2 QPSK, 3/4 QPSK, 1/2 16-QAM, 3/4 16-QAM, and 7/8 16- QAM, with a theoretical maximum bit rate of $\approx$ 4.8 Gbps and $\approx$ 3 Gbps for SC and OFDM, respectively.

4.2 Experimental Results

The THz front-ends (Section 2) accept/generate an IF as the input/output of the transceiver system. Therefore, the NI back-ends used in IF mode to interface with the 220-240 GHz and 120-140 GHz front-ends. The 1 THz front-end has limited transmit power (30 μW max transmit power) and thus needs high sensitivity data converters at the receiver-end to recover the signals. The NI ADCs have a lower dynamic range with higher minimum sensitivity. Thus, currently, the NI back-end is not usable with the 1 THz front-ends at even at much smaller transmission distances.

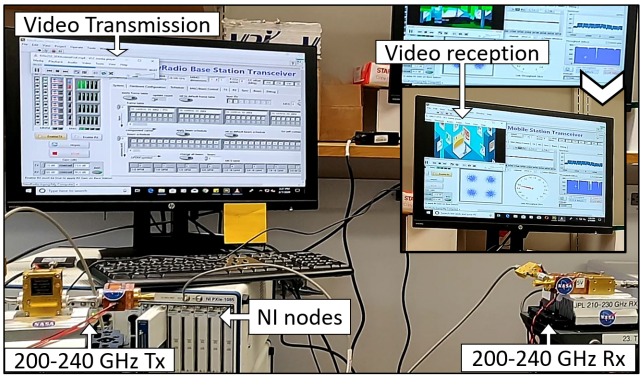


Figure 6. NI back-ends used with 220-240 GHz front-ends for real-time data transmission.

We used the NI nodes to generate a 10.5 GHz IF to the front-ends and experimented data-transmission using the MCSs 1/2 QPSK and 1/2 16-QAM. The experiments yielded 720 Mbps and 840 Mpbs throughput, for QPSK and 16-QAM modulations, respectively (in the multi-carrier mode). We have also demonstrated successful end-to-end transmission of a video clip using the NI back-end and the 240 GHz front-ends. Figure 6 illustrates a snapshot of the real-time experiment. Similarly, we used the NI back-end to generate multi-carrier modulated streams that were then upconverted to an IF at 10.5 GHz and interfaced to the 120-140 GHz front-ends. The transmitter and receiver were spaced 40 cm apart and MCSs 1/5 BPSK, 1/2 QPSK and 1/2 16-QAM were tested. The recorded throughput were 117, 416, and 750 Mbps for the above MCSs, respectively, whereas the theoretical expected rates were 118, 1188, and 2674 Mbps, respectively.

Since the NI system has been designed mainly for mmWave front-ends, the frame-structure, synchronization mechanisms, and phase noise compensation algorithms are not tailored for the THz front-ends. This makes the NI back-ends sub-optimal to use with the THz-front-ends out of the box which also leads to the performance degradation reported in the above experiments. The frame structure, phase noise compensation, and synchronization blocks have to be customized for the application.

5 Xilinx RFSoC based Signal Processing Back-End

5.1 System Overview and Specifications

Given the bandwidth limitation of the NI back-end, we envision a real-time multi-channel baseband digital signal processing engine (DSP) able to independently manipulate and, when required, jointly aggregate multi-GHz-wide channels

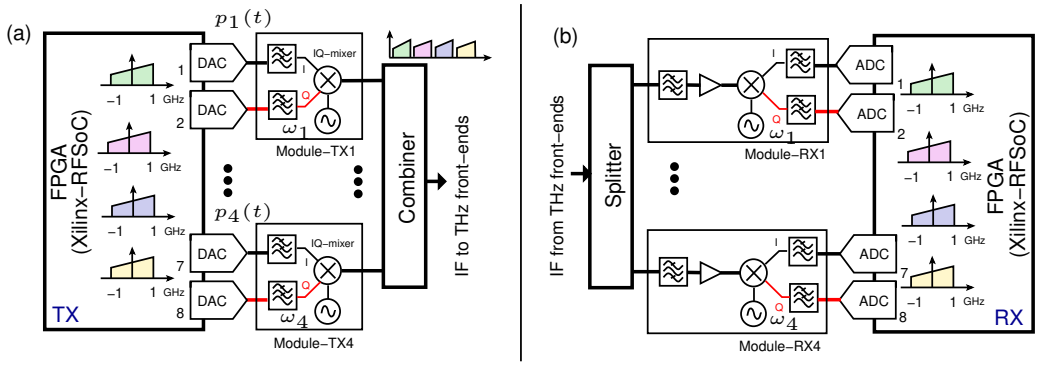


Figure 7. Overview architecture of the RFSoC based real-time back-end; (a) transmitter side, (b) receiver-side.

that can be up/down-converted by the aforementioned front-ends spanning across multiple THz frequency bands. Such an effort will enable real-time communication at these frequency bands which is a limitation of our current testbed. We believe that a possible approach for realizing ultrabroadband signals with digital back-ends would be to use data links consisting of multiple frequency multiplexed radio channels which would allow digital processors to process slower manageable bandwidths. Using multiple ADC/DAC chips to interface sampled data to the processor through high-speed interfaces is infeasible due to prohibitive hardware complexity and power consumption. Therefore, we propose a back-end system where a system-on-a-chip (SoC) with multiple data converters (preferably supporting GSps rates) integrated on the same chip alongside the digital logic for reconfigurable SDR. Each low-bandwidth channel is processed on its own digital back-end leading to a multi-channel SDR processor. For this, we exploit the Xilinx radio-frequency SoCs (RFSoCs) to enable low size-weight-and-power (SWaP) realization of frequency multiplexed multichannel SDRs. These SoC integrations eliminate the large number of external interfaces required for interfacing analog signals and thereby facilitate deployment of higher number of channels in a smaller foot print with greatly reduced power consumption. Thus, the system that is proposed (which is being implemented), will leverage the RFSoC chips [10] for implementing digital back-ends at both the transmitter and the receiver side.

The Xilinx RFSoCs were released a few years back and the device's first generation supported up to 16 DACs and ADCs that can be clocked up to 6.55 GSps and 4.096 GSps respectively. Up to now these devices have been primarily used for realizing MIMO and phased array solutions for 5G mmWave applications to interface multi-antenna systems with digital back-end [5, 18, 28, 29]. Instead, we propose to use the on-chip multiple DACs and ADCs available in the RFSoCs to multiplex multiple low-bandwidth slower channels to process a multichannel high bandwidth signal to support real-time wireless links at tens to hundreds of Gbps. The overview architecture of the proposed real-time back-end processing system is shown in Figure 7. The current implementation uses the ZCU111 RFSoC evaluation boards which feature the 1st generation Xilinx ZU29DR RFSoC chips. This particular chip supports 8 DACs and 8 ADCs which can be clocked at a max rate of 6.55 GSps and 4.096 GSps, respectively. Thus, ideally supporting 2.048 GHz ×8 = 16.4 GHz of total bandwidth at the ADCs and 3.27 GHz ×8 = 26.2 GHz at the DACs. Each DAC has a 14-bit resolution whereas the ADCs come with 12-bit precision. The programmable logic (PL) part or the FPGA fabric of the chip comprises of 930K logic cells and over 4K DSP slices, along with 60.5 Mb of block RAM memory. The RFSoC also has four ARM Cortex-A53 cores and two ARM Cortex-R5 cores hardened which can be used to run real-time OSs, or bare metal application for real-time communication/processing with PL. The ZU29DR RFSoC chip also come with eight hardened soft-decision forward error correction (SD-FECs) IP blocks [10]. These IPs support LDPC encoding/decoding and Turbo decoding. Such integrations enable low latency, multi-Gbps data rates compared to soft cores and saves FPGA resources for other logic implementation. The ZCU111 platform in particular supports, 4 SFP+ optical connections to PL to support data high data rate in and out streaming. One Gbps Ethernet connectivity has been provided for APU side as high speed connectivity through APU.

For the full system design shown in Figure 7, minimum of maximum clockable frequencies at both DACs and ADCS, which is 4.096 GSps will be used. To relax the analog filtering requirements of both anti-imaging and anti-aliasing filters, 2× interpolation/decimation is used at DACs and ADCs, respectively. As shown in Figure 7(a), 2 DACs (out of 8) are used to generate/process a single channel (complex baseband) of 2.048 GHz at the transmitter. Thus, in total 4 such baseband channels can be accommodated (given that 4× the logic can fit in to the PL, which will be mostly critical at the receiver-side). The architecture of the receiver-side baseband processing back-end is similar to the transmitter-side and is shown in Figure 7(b). Each donwconverted baseband channel will be quadrature sampled using 2 ADCs at 4.096 GHz and will be decimated 2× before processing.

Analog RF Circuits. At the transmitter, each baseband channel has to be properly frequency multiplexed to form

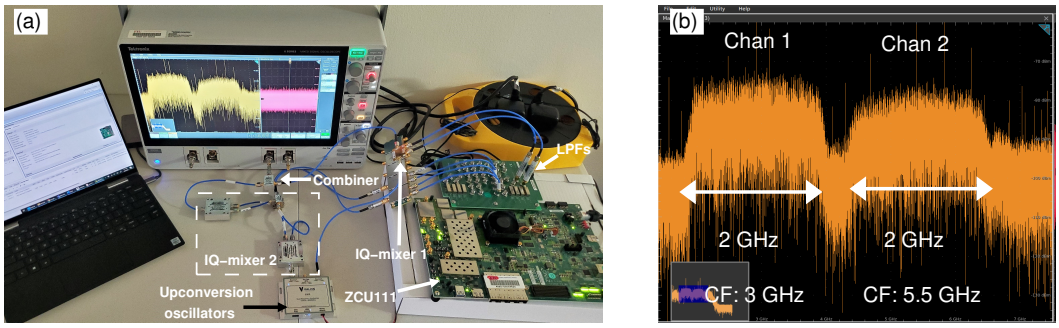


Figure 8. (a) Experimental prototype of the proposed transmitter-side back-end. (b) Scope capture of the output at the combiner which aggregates 4 GHz of bandwidth by multiplexing two 2 GHz channels (centered at 3 and 5.5 GHz); Xilinx ZCU111 board is used to generate the 2 GHz channels using 4 of the DACs out of 8 (CF denotes the center frequency).

an aggregated fat IF output to be fed in to the THz front-ends. This will be achieved through a set of IQ-mixers, that will upconvert the baseband channels to different IF carriers ω_k, $k \in \{1, 2, 3, 4\}$, where 2 GHz $< \omega_k <$ 18 GHz. The ω_k frequencies will be carefully chosen to allow a sufficient guard between the channels and avoid inter-channel harmonic distortions. The upconverted frequency multiplexed channels will ultimately be combined using a wideband combiner to form an aggregated IF that will be sent to THz front-ends.

The receiver-side will be designed in a similar fashion to undo the aggregated channels in the received IF. To achieve this, the received IF will be split into 4. Then each output will be subjected to a bandpass filtering at each ω_k center frequency to filter out each 2 GHz wide channel. A set of amplifiers will be used to maintain the required cascaded gain in each channel. The separated IF signals centered at different ω_k frequencies then will be direct converted back to baseband using a set of IQ mixers with local oscillators tuned to ω_k. The downconverted IQ channels will be lowpass filtered and sampled separately in to the RFSoC.

Digital Baseband Processing. Although the data converters of the RFSoCs can be clocked at speeds exceeding 4 GHz, the maximum rate the PL fabric can be clocked is about an order of magnitude less than the maximum sampling rates. Thus, efficient polyphase digital circuit architectures are required for processing such high bandwidth signals. Therefore, digital circuits are designed in a polyphase manner for PHY processing while leveraging the maximum bandwidth supported by data converters.

PHY Layer Specifications. For the initial implementation, the PHY layer is chosen to be based on OFDM. Due to the ultra-wide bandwidth supported by the front-ends of the current testbeds, a stronger contribution to the overall channel frequency selectivity comes from the hardware electronics. Initial measurements using the 120 GHz front-ends (discussed in section 2.1) were carried out to determine the sub-carrier spacing such that the subchannels can be regarded frequency flat. The measurement showed that this is met for bandwidths < 50 MHz per subcarrier and thus an FFT size of 64 was used to design the PHY layer. Since the baseband (including the OFDM processor) is clocked at 2.048 GHz, subcarrier spacing for the implementation is 32 MHz. The digital cores are designed to support up to 64-QAM modulations with the option of adaptive modulations at subcarrier-level. PHY layer frame structure has been implemented with close resemblance to 802.11a standard due to the choice of 64-point FFT size.

5.2 Prototype System and Preliminary Experimental Results

A prototype system having the architecture discussed above is currently being developed. To start with, the transmitter side has been implemented using the Xilinx ZCU111 board. The DACs are driven at 4.096 GSps with 2× upsampling with FPGA circuits running effectively at 2.048 GSps. A 16-phase polyphase digital architecture is used to implement the PHY processing. For demonstration purpose, two baseband channels were generated from the RFSoC and two IQ mixers with LOs operating at $\omega_1 = 3$ GHz and $\omega_2 = 5.5$ GHz were used to up convert the signals. The two 2 GHz channels were then aggregated to form a 4 GHz IF using a 2-way combiner.

Figure 8(a) shows the transmitter platform that has been built. Figure 8(b) shows the frequency domain plot of the combiner IF output having 4 GHz of aggregated bandwidth where each channel having 2 GHz of bandwidth are combined (centered at 3 GHz and 5.5 GHz). System is currently being extended to 4 channels to support 8 GHz of bandwidth at the transmitter side leveraging all 8 DACs of the ZU28DR chip. RFSoC based receiver-side processing node is also being developed along with the multi-channel demultiplexing front-end to bring the IF channels to baseband.

6 Conclusion

For many years, THz experimental research has been focused on characterizing the THz channel as well as testing and demonstrating new THz devices, usually for implementing the traditional communication techniques. Moving forward, non-traditional communication and networking solutions

tailored to the capabilities of THz devices and the peculiarities of the THz channel that can be found in the related literature need to be experimentally tested and refined. The experimental platform and signal processing backend presented in this paper enables such research. We aim to not only utilize, maintain, and enhance the current platform, but also to open the platform to the broader wireless communication research community.

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