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Asymmetrically Engineered Nanoscale Transistors for On-Demand Sourcing of Terahertz Plasmons

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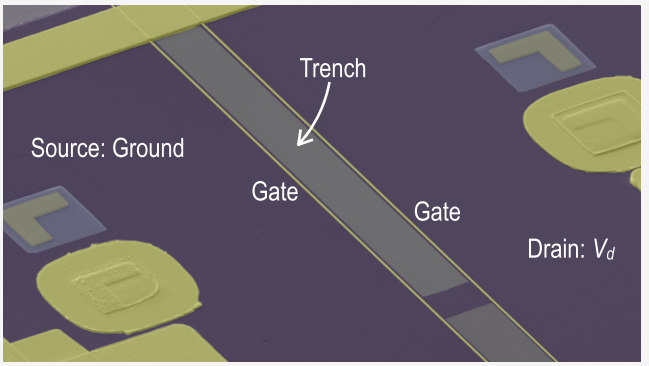
ABSTRACT: Terahertz (THz) plasma oscillations represent a potential path to implement ultrafast electronic devices and circuits. Here, we present an approach to generate on-chip THz signals that relies on plasma-wave stabilization in nanoscale transistors with specific structural asymmetry. A hydrodynamic treatment shows how the transistor asymmetry supports plasma-wave amplification, giving rise to pronounced negative differential conductance (NDC). A demonstration of these behaviors is provided in InGaAs high-mobility transistors, which exhibit NDC in accordance with their designed asymmetry. The NDC onsets once the drift velocity in the channel reaches a threshold value, triggering the initial plasma instability. We also show how this feature can be made to persist beyond room temperature (to at least 75 °C), when the gating is configured to facilitate a transition between the hydrodynamic and ballistic regimes (of electron–electron transport). Our findings represent a significant step forward for efforts to develop active components for THz electronics.



KEYWORDS: *terahertz transistors, plasmonics, plasma waves, negative differential conductance, Dyakonov–Shur instability*

Plasma oscillations in semiconductors involve the collective motion of free carriers at terahertz (THz) frequencies, making them appealing for use in high-frequency, 6G, and beyond communication schemes.[1,2] The possibility of realizing sustained plasma oscillations in high-electron-mobility transistors (HEMTs) was predicted by Dyakonov and Shur,[3] who used a hydrodynamic model to analyze charge dynamics in a transistor channel. Their treatment assumed weak impurity and phonon scattering, and the diffusive limit of electron interactions ($\tau_{e-e} < \tau_T < \tau$, where τ_{e-e} is the electron–electron scattering time, τ_T is the transit time across the transistor, and τ is the momentum relaxation time). In this framework, the authors predicted that a steady-state current through the transistor can become unstable to plasma wave generation, a phenomenon known as the Dyakonov–Shur (DS) instability. Subsequently, Shur and colleagues extended[4] these arguments beyond the hydrodynamic limit, predicting that the DS instability can also arise in the collisionless—or ballistic—regime, for which τ_{e-e} is now longer than τ_T.

In either the hydrodynamic or collisionless regimes, the spontaneous onset of plasma oscillations via the DS mechanism is only expected in transistors with very specific structural asymmetry. Dyakonov and Shur[3] considered a geometry in which the (ac) impedance (Z_s) between the source and gate is zero (i.e., a short circuit), while that between the gate and drain (Z_d) is infinite (i.e., an open circuit for which $Z_d/Z_s \rightarrow \infty$). This impedance mismatch allows plasma waves generated under a static drain bias (V_d) to grow exponentially as they travel back and forth below the gate that defines a plasmonic cavity and thereby generates an instability in the 2D plasma. Eventually, these motions stabilize as a sustained, periodic plasma mode.[5−8]

While the DS instability has been explored in various experimental geometries,[9−18] the issue of the required impedance mismatch, and its impact on the characteristics of the instability, has not been systematically addressed. In early work,[9] for example, performed on commercial transistors, the ideal boundary conditions were approximated by physically shorting the source to the gate and driving the transistor into saturation (forming a pinched-off region near the drain). In subsequent work,[13] customized HEMT designs in which the gate was positioned closer to the source than the drain were

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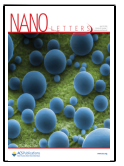

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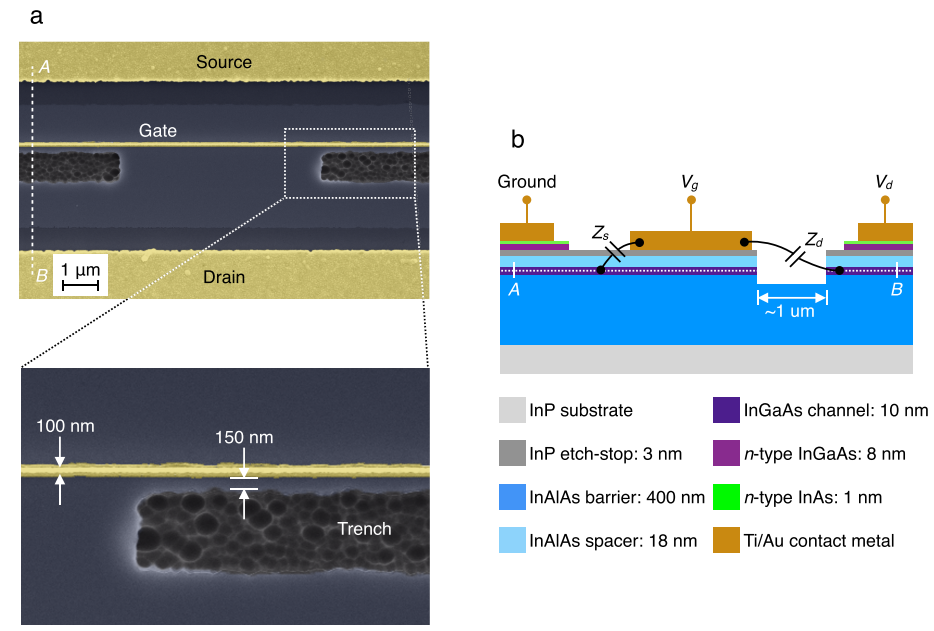

Figure 1. (a) Colorized electron micrographs of a gated 2DEG plasmonic cavity. The full mesa width is 115 μm, and the images show an expanded view around the center region where both the etched trench and unetched region can be seen. (b) Schematic (not to scale) of the layer structure of our devices. The image represents the structure as seen along the dashed line *AB* in panel a. Silicon delta-doping layers are inserted in the upper (8 nm) InGaAs layer, where the source and drain contacts (at Ground and V_d, respectively) are formed, and in the 18 nm InAlAs spacer. An additional delta-doped layer is also present at the interface between the InGaAs and the InP etch-stop layer. Also denoted in the figure are the capacitive impedances between the gate and the source (Z_s) and the gate and the drain (Z_d). Z_s is governed by the distance between the 2DEG and the gate (~21 nm), while Z_d is essentially determined by the distance between the gate and 2DEG on the other side of the trench (~1 μm).

fabricated, effectively realizing the asymmetric boundary conditions necessary for the DS instability.[19] While these devices were found to emit tunable THz radiation in accordance with the DS instability, the emitted THz power was weak (~μW), raising the question of how the electrical power supplied to the device was dissipated.

In this Letter, we present a novel scheme for engineering the boundary conditions in HEMT devices, realizing the strong asymmetry required for the DS instability. Our approach involves the precise placement of the nanoscale gate under which the plasma motions stabilize, in close proximity to an etched trench that ensures the high impedance needed[3] at the drain (Figure 1a,b). The static transistor curves of these devices exhibit negative differential conductance (NDC) that has previously been connected to the onset of the DS instability.[7,9,13] Consistent with the engineered asymmetry in our devices, the NDC is only observed under forward bias ($V_d > 0$). Reversing the bias polarity, on the other hand, reverses the roles of the source and drain (i.e., $Z_d/Z_s \to 0$), and we consequently find no evidence of the DS instability. To the best of our knowledge, this is the first demonstration of using nanoscale structuring to engineer the boundary conditions required for the DS instability. In temperature-dependent studies, we demonstrate how control of the electron density in the plasmonic cavity below the gate can extend the survival of the instability beyond room temperature. We suggest that this behavior arises from a corresponding crossover between the hydrodynamic and ballistic regimes of electron−electron scattering. Finally, we address the issue of the weak emission associated with the plasma mode by demonstrating theoretically that most of the electrical power supplied to the transistor should be consumed while sustaining its periodic charge motions, rather than as a loss through the emission of radiation. In this sense, our results suggest that the DS instability can better serve as an on-chip source of THz plasmonic signals rather than of free-space radiation.

To better understand the conditions under which plasma waves can be excited in an HEMT channel, we have modeled transport in the simple transistor geometry shown schematically in Figure 2a. In these calculations, we numerically solve the self-consistent system of hydrodynamic equations for the electron plasma, along with the Maxwell equations. The computations were performed using the finite-difference-time-domain package supported in COMSOL's Multiphysics simulation software, allowing for simultaneous determination of both the hydrodynamic and the Maxwell equations in the time domain[8] (Supporting Information, Section S1). In this way, we calculate the impact of plasma oscillations on the dc characteristics of a two-dimensional electron gas (2DEG)-based transistor in the linear (ohmic) limit. To realize sustained plasma oscillations, the ideal boundary conditions $Z_s = 0$ and $Z_d = \infty$ [see Figure 2a] were imposed by hand in the model.

The main panel of Figure 2b shows computed transistor (I_d−V_d) curves at various electron densities (n_o). The insets plot the temporal variation of the induced plasmonic current in the electron fluid, resulting from an instantaneous current perturbation at different values of V_d (see caption). For positive drain bias, corresponding to normal device operation, plasma excitations can develop in the channel due to the DS instability. The excitation is sustainable over a density-dependent range of bias ($V_1(n_o) < V_d < V_2(n_o)$), outside of which the plasmons decay via collisional damping. For negative V_d, however, there is no indication of sustained plasmons; excitations instead always decay rapidly, in agreement with linear analysis.[3] In the main panel of Figure 2b, we show that, at positive bias, the transistor curves exhibit pronounced NDC for a wide range of density and V_d. We find that the NDC

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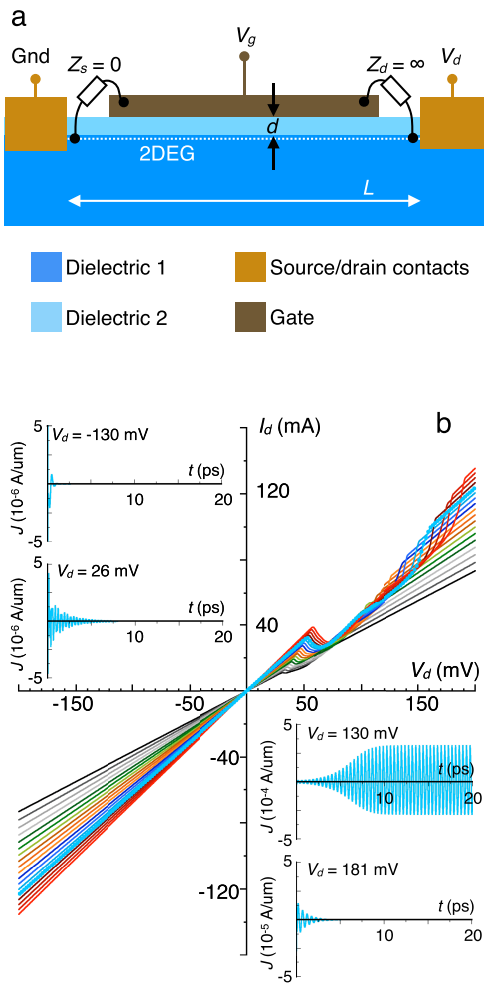

Figure 2. (a) Schematic illustration of the transistor geometry utilized in the numerical simulations. The ac impedances $Z_s = 0$ and $Z_d = \infty$ are externally imposed boundary conditions in the calculations. (b) The main panel shows calculated I_d−V_d curves, obtained within our model for the plasmonic instability. Moving from the lowermost (black) to the uppermost (red) curve at V_d = 200 mV, the electron density in the channel is increased from 3.5×10^{11} to 1.2×10^{12} cm^{-2}, in increments of 0.5×10^{11} cm^{-2}. The four insets show the calculated time-dependent variation of the current at the source, resulting from the application of instantaneous current perturbations at the indicated values of V_d and for $n_o = 1.0 \times 10^{12}$ cm^{-2}. Sustained THz oscillations are observed when V_d = 130 mV, lying within the region of NDC (see the I_d−V_d curve with solid symbols).

occurs over the parameter space for which the transistor undergoes sustained plasma oscillations and is consequently absent at negative V_d, due to the aforementioned damping.

For an experimental demonstration of the predictions above, we realize plasmonic cavities with asymmetric coupling by fabricating transistors in InGaAs/InAlAs heterostructures grown by molecular-beam epitaxy on InP substrates.[20] The layer structure of this material is shown in Figure 1b, in which the 2DEG in the $In_{0.8}Ga_{0.2}As$ was formed by Si delta-doping and was located 21 nm below an InP etch-stop layer that formed the top surface of the devices. Hall measurements of ungated sections of 2DEG, without any trench, were used to determine an electron density of $\sim 2.8 \times 10^{12}$ cm^{-2} (Supporting Information, Section S2). The mobility (μ) and mean-free path (l_{mfp}) of the 2DEG were μ = 84100/62300/13400 cm^2/(V·s) and l_{mfp} = 2.3/1.7/0.4 μm at 3/77/300 K, respectively. While l_{mfp} was therefore longer than the gate length over the entire range of temperature studied, this should only be taken as a qualitative indicator since this length scale pertains to low-field, single-particle transport rather than the collective plasmonic response at a large drain bias. Nonetheless, the values of μ and l_{mfp} should be considered indicative of the high quality of our devices. Fabrication of the devices involved a process in which a trench was formed on the drain side of the device mesa by electron-beam lithography and wet etching (in dilute HCl and H_2O_2). Electron-beam lithography and lift-off were used to create the nanoscale (Ti/Au: 20-/150 nm) metallic gate (~100 nm long), which was deposited over the entire width (~115 μm) of the 2DEG mesa. The gate was precisely aligned (within ~150 nm) with one edge of the trench. A representative device is shown in Figure 1a, in which the gate-defined plasmonic cavity is directly connected to a large area of 2DEG that functions as the source and which provides a relatively small (capacitive) gate-to-source ac impedance (see Figure 1b). On the other side, the extreme proximity (~150 nm) of the gate to the etched trench introduces a large gate-to-drain impedance that is essentially set by the trench width (i.e., $Z_d/Z_s \gg 1$). Although this impedance is maintained over almost the full mesa width, a conducting aperture, several microns wide, is introduced near the center of the trench (as shown in Figure 1a). This feature is needed to enable the steady-state flow of (dc) current from source to drain, a prerequisite[3] for triggering the DS instability. As such, the plasmonic excitation is assumed to occur in the gated regions on either side of the aperture rather than in the vicinity of the aperture itself. Although we did not systematically investigate the impact of the aperture geometry on the resulting transistor characteristics, its width was chosen to be sufficiently large (~5 μm) to ensure that its contribution to the overall source-drain resistance was smaller than that of the gated region.

Devices were wire-bonded in a chip package and mounted in the light-tight vacuum enclosure of a variable temperature (3−500 K) cryostat. Their transfer (I_d−V_g; V_d = 100 mV) and transistor (I_d−V_d) curves were measured with a Keithley 2400 dc source-measure unit. For consistency, we focus in Figures 2 and 3 on the results obtained in a comprehensive study of a single device. We emphasize, however, that the key behaviors reported in this work were reproduced consistently in studies of numerous devices. We demonstrate this in Section S4 of the Supporting Information, where we provide further examples of the NDC in other devices.

The main panel of Figure 3a shows transistor curves measured at various gate voltages and for drain biases of both polarities. At V_g = 0 V, the carrier density underneath the gate should be (almost) the same as in the 2DEG (2.8×10^{12} cm^2), and the plasmon cavity will not be formed. The resulting transistor curve is unremarkable and largely symmetric around V_d = 0, exhibiting linear behavior at a small bias ($|V_d| < 0.5$ V) and a saturation at higher voltages, behaviors that are well established for high-electron mobility transistors.[21−24] On applying a large negative gate voltage (-4.50 V $\le V_g \le -2.50$ V), in contrast, the current is quenched over a wide region around a zero drain bias. Such behavior indicates that the strong repulsive potential generated by the gate has locally depleted the 2DEG, driving the conduction-band edge above the Fermi level. This pinch-off condition can be overcome if sufficient V_d is applied to generate drain-induced barrier lowering[25] (DIBL). Once this occurs, the resulting variation of

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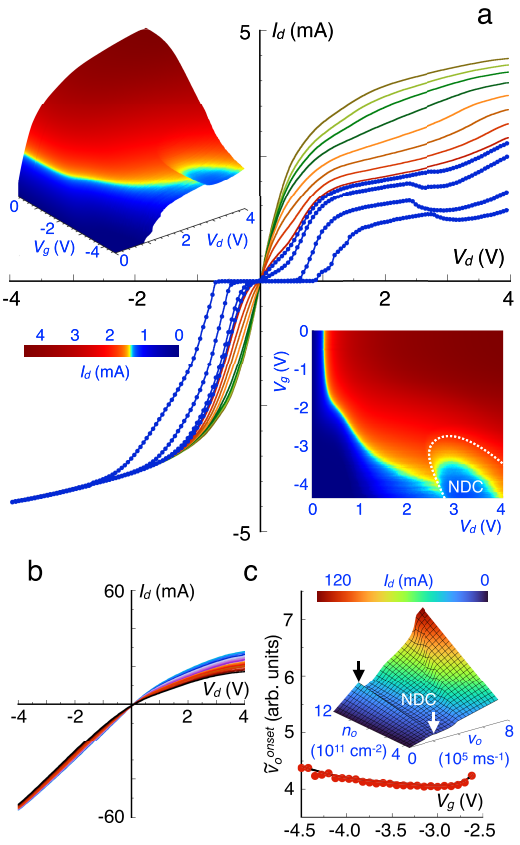

Figure 3. (a) The main panel shows transistor curves measured at 3 K in a representative device such as that of Figure 1a. From top to bottom at V_d = 4 V, the different curves correspond to V_g = 0, −0.50, −1.00, −1.25, −1.50, −1.75, −2.00, −2.25, −2.50, −2.60, −2.80, −3.50, and −4.50 V. Curves plotted with filled symbols exhibit NDC at a positive drain bias that is absent upon reversal of the polarity of V_d. The three- (upper-left inset) and two- (lower-right inset) dimensional color contours show the detailed evolution of drain current with V_g and V_d. Both contours use the calibration scale included as the lower-left inset of the main panel. In the lower-right inset, the white-dotted line encloses the range of NDC. (b) Absence of NDC in a symmetric device (also at 3 K), featuring only a narrow gate and no etched trench (i.e., $Z_s = Z_d$). From top to bottom at V_d = 4 V, the different curves correspond to V_g = −2.50, −2.60, −2.70, −2.80, −2.90, −3.00, −3.10, −3.20, −3.30, −3.40, −3.50, −3.60, −3.70, −3.80, −3.90, and −4.00 V. (c) Variation of the effective drift velocity at the onset of NDC ($\tilde{v}_o^{onset}$), obtained from the measurements of Figure 2a using the approach described in Section S3 of the Supporting Information. The inset plots the calculated drain current as a function of n_o and v_o. Over the entire range of density plotted, NDC onsets once v_o reaches a value of ∼2 × 10^5 ms^{-1} (see arrows).

the current in Figure 3a is strongly dependent upon the polarity of V_d, with pronounced NDC being observed at a positive bias that is absent at negative V_d. Comparison of Figures 2b and 3a reveals a common feature, namely, NDC that is present for positive V_d only and which our theory connects to the DS instability. With regard to the differences between the experiment and theory, we first note that, since our model is based upon a linear formulation of conduction, Figure 2b does not capture the high-field[26] current saturation seen in Figure 3a. Nonetheless, we emphasize that the DS instability is not dependent upon an assumption of linear conduction but can also occur in the nonlinear regime.[9] The only critical condition for this effect is that the drift velocity should exceed some required threshold (see below). Second, it is apparent that the values of V_d at which NDC occurs in Figure 2b are smaller than those in the experiment. This too may be related to the onset of current saturation in the experiment. In the presence of the saturation, the channel resistance increases with increasing drain voltage, requiring a larger voltage yet to achieve the aforementioned drift-velocity threshold. The difference between theory and experiment may also partially be because the cavity is initially pinched-off in the experiment so that the drain bias must first generate sufficient DIBL before conduction begins. While a more sophisticated model of transistor action, which accounts for the nonlinear effects that arise in actual devices, might better describe the full experimental behavior, our calculations capture the NDC that arises from plasmonic excitation. In Figure 3b, we demonstrate that the structural asymmetry of our devices is essential to the manifestation of NDC, by plotting transistor curves for a device without a trench. This device is structurally symmetrical ($Z_s \approx Z_d$) and shows no NDC, consistent with the idea that sustained plasmons should not exist in this geometry.

The DS instability is predicted to exhibit threshold character, onsetting[3] once the drift velocity increases sufficiently that asymmetric reflection at opposite ends of the gate-defined cavity causes plasma-wave amplification to exceed any damping. An example of this thresholding is shown in the inset in Figure 3c, where we plot the calculated variation of I_d as a function of n_o and drift velocity (v_o). For a wide range of densities, NDC onsets once the velocity reaches a fixed threshold (∼2 × 10^5 ms^{-1}), determined[3] by the gate length (L) and the scattering time of plasmons (τ) in the channel ($v_o \approx L/\tau$). Evidence of thresholding is also found experimentally, as we describe in greater detail in Section S3 of the Supporting Information where we define an effective drift velocity at the onset of NDC ($\tilde{v}_o^{onset}$). In Figure 3c, we show that $\tilde{v}_o^{onset}$ is almost constant over a wide range of V_g, consistent with a threshold effect. It is the existence of this threshold condition that underpins the different variations of the NDC found in our model (Figure 2b) and in experiments (Figure 3a). In the case of the former, the density in the channel is taken to be independent of V_d, and the onset of NDC therefore shifts continuously to a larger drain bias with increasing density (see Supporting Information, Section S1). The experimental situation is more complex. The density under the gate depends not only on V_g but also on V_d. Nonetheless, estimation of $\tilde{v}_o^{onset}$ from the experimental data yields an almost constant value, consistent with the DS mechanism.

The measurements of Figure 3 were obtained at 3 K, where phonon scattering is suppressed, and the long mean-free path of the 2DEG should support sustained plasmons. This situation should change at higher temperatures, where increased phonon scattering should damp the plasmons by adding "extrinsic friction" to the electron fluid.[3] In Figure 4a, we plot transistor curves (I_d (V_d)) at various temperatures for a fixed gate voltage V_g = −3.50 V. Here, the 2DEG under the gate is fully pinched-off at V_d = 0, and the NDC persists to (even strengthens at) the highest measured temperature of 290 K. In Figure 4b–d, we use color contours to show the temperature-dependent evolution of the NDC at V_g = −2.30, −2.70, and −3.10 V, respectively. In panel (b), the electron gas is undepleted under the gate at V_d = 0; the NDC weakens relatively quickly with increasing temperature and is suppressed completely by 60 K. This wash-out temperature is increased to 150 K in panel (c), while in panel (d) the NDC is even observed near room temperature (∼250 K). Indeed, we

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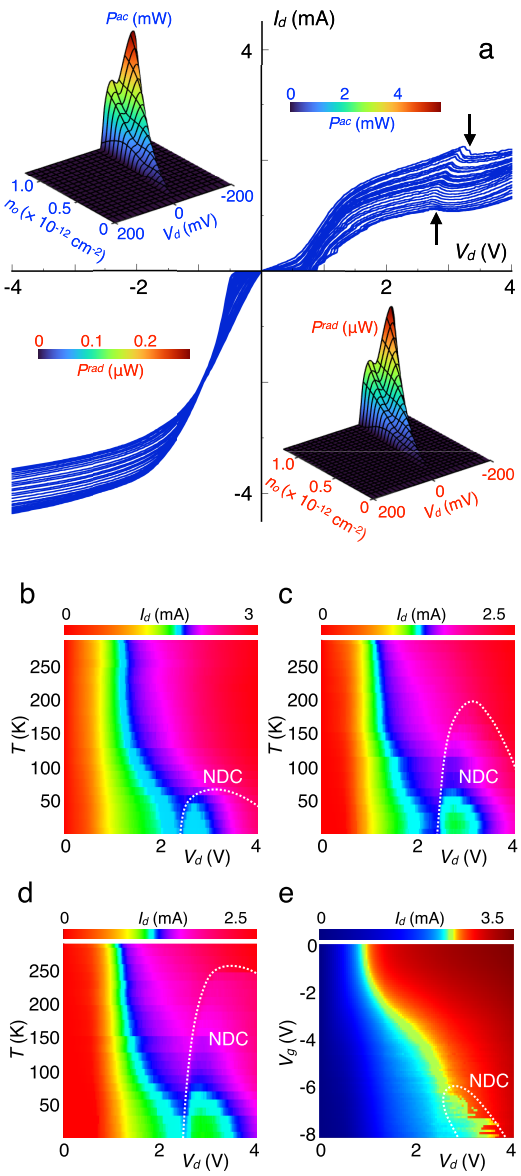

Figure 4. (a) The main panel shows transistor curves measured at V_g = −3.50 V, at various temperatures from 10 to 290 K. Referring to the data at V_d = +4 V, the temperature is increased in 10 K increments from bottom to top. Arrows denote onset of NDC at 10 K and 290 K. The insets plot calculated energy losses due to plasmon-induced heating (P^{ac}, upper-left inset with color scale defined in the upper-right quadrant) and radiation (P^{rad}, lower-right inset with color scale defined in the lower-left quadrant). (b−d) Contours plotting variation of I_d (V_d, T) at fixed gate voltages of V_g = −2.30 V, −2.70 V, and −3.10 V, respectively.(e) Contours plotting variation of I_d (V_d, V_g) at 350 K. Color scale for panels b−d is denoted at the top of each contour.

have even found that the NDC can persist beyond room temperature, as shown in Figure 4e. In contrast to panels b−d, this contour compiles transfer curves (I_d (V_g)) at 350 K and exhibits NDC at the most-negative gate voltages (V_g < −6 V; note how the current is suppressed near V_d = 0 for these curves, indicative of the strong depletion generated initially by the gate bias).

The DS instability was originally derived[3] for strong electron−electron scattering, a limit not easily reached (due to Pauli blocking) in strongly degenerate 2DEGs. While the nondegenerate limit can be approached by increasing temperature, this typically comes at the cost of increased phonon scattering; it is this contradictory, competitive character that has long rendered the observation of hydrodynamic effects in semiconductors challenging.[27] Conversely, realizing hydrodynamic phenomena requires innovative strategies. Current heating has been used, for example, to selectively increase the carrier temperature separate from the lattice.[28] This allows the electron system to be driven toward the nondegenerate state needed for efficient electron−electron scattering, while leaving electron−phonon scattering unchanged. In our work, we alternatively approach the nondegenerate state by locally reducing the carrier density below the gate. This provides an optimal means to reach the hydrodynamic limit, by first pinching-off the channel (at low temperatures) and then allowing a nondegenerate population of carriers to be introduced via a combination of thermal activation and DIBL.

The different temperature-dependent behaviors shown in Figure 4 are consistent with the plasmonic origins of the NDC. First, it can be seen in Figure 4a that the onset of the NDC shifts to larger V_d values as the temperature is increased, and electron−phonon scattering consequently becomes stronger. To overcome the damping of plasmons by phonons, a larger drain bias is then needed to reach the instability threshold. Second, one can mitigate the adverse impact of phonon scattering on the plasma oscillations by decreasing their damping due to the finite viscosity (or "intrinsic friction") of the electron fluid.[29] This can be achieved by driving the fluid toward a noninteracting, gas-like state, under sufficient reduction of the electron density underneath the gate. This interpretation is consistent with Figure 4b−d, which show that the instability washes out at higher temperatures as V_g is made more negative and intrinsic friction is reduced. Ultimately, this procedure may even drive the electron plasma into the collisionless−ballistic−limit, provided phonon scattering remains sufficiently weak. (Recall that the electron mean-free path is much larger than the cavity length, even at room temperature; see Supporting Information.) The DS instability is still expected in the ballistic limit, exhibiting the same exponential growth of the plasma waves as in the hydrodynamic limit.[4] Such a crossover from the hydrodynamic to the collisionless regime may be responsible for the strengthening of the NDC with increasing temperature, seen in Figure 4a, and the observation (Figure 4e) that NDC persists at 350 K for the most-negative gate voltages.

With the plasmonic mode stabilized, energy supplied from the external circuit is balanced by losses due to plasmon damping, which primarily occurs via (i) Joule heating of the 2DEG by the plasmon electric field and (ii) radiation losses. In the insets in Figure 4a, we plot the power losses to heating (P^{ac}) and radiation (P^{rad}), calculated (Supporting Information, Section S1) for the same parameters as in Figure 2. The range over which these losses are significant is well correlated to that where NDC is observed in Figure 2b, reflecting the origins of P^{ac}/P^{rad} in the DS instability. While the calculations confirm the existence of emission (P^{rad} < μW) from the plasmonic mode, they also show that this is some four orders of magnitude weaker than P^{ac}. In other words, the DS instability represents a more efficient means for the on-chip sourcing of THz plasmons rather than for the emission of free-space THz radiation. One way in which the radiated power might be

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increased using these devices is by integrating them into arrays with large numbers of plasmonic transistors.

The results presented here provide strong evidence for the stabilization of sustained plasmonic oscillations in gated 2DEGs. While the evidence for these oscillations is indirect, in the sense that it is manifested in the static (dc) characteristics of the devices, future work could explore real-time signatures of these oscillations by performing transient measurements on the nanosecond scale.[30,31] Although such transients are still much longer than the picosecond period of the expected oscillations, they are expected to be shorter than the characteristic time scale for Joule heating of the devices.[31] As such, these transients can therefore allow the long-time dynamics of the plasma oscillations to be explored.[32]

Although the results presented here have been obtained by implementing transistors in a specific III−V system, we emphasize that our strategy of realizing asymmetric transistor coupling should be amenable to use with other materials, most notably with graphene.[33−39] Another important point is that, by demonstrating the connections of the observed NDC to the deliberate asymmetry ($Z_s \ll Z_d$) of our devices, we can exclude other known sources of NDC. The Gunn effect, for example, arises from scattering between the different conduction-band valleys of the host semiconductor and has long been exploited as the source of stable microwave (rather than THz) signals.[40] Similarly, real-space transfer between different layers of the heterostructure is another effect that is known to give rise to NDC.[41,42] If relevant, however, these effects should be manifested in symmetric devices (recall Figure 3b) and should also be observed for *both* polarities of V_d. In contrast, as we illustrate in Figure 3a, even though the overall magnitude of the current is similar at positive and negative drain biases (for all gate voltages), NDC is only present at a positive bias. The asymmetric plasmonic devices that we have implemented have considerable potential for use as local oscillators that may be used to source high-frequency on-chip signals for future communication systems.[1,2] By integrating them with graphene and other two-dimensional materials, they may also even be used to launch plasmons into such layers for modulation, radiation, and, ultimately, free-space communication.[43]

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.1c04515.

Details of the theoretical model developed to describe the plasma-wave dynamics in a high-mobility transistor; the results of electrical characterization of the two-dimensional electron gas in the $In_{0.8}Ga_{0.2}As/In_{0.52}Al_{0.48}As$ heterostructure, and further demonstrations and characterization of the negative differential conductance in the experiments (PDF)

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Notes

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