D-Band SDR with 64 GHz B/W on COTS Chiplets

Buddhipriya Gayanath[(1)], Kasun Karunanayake[(1)], Hussam Mohammad[(2)],
Satheesh Bojja Venkatakrishnan[(1)], Elias A Alwan[(1)], Josep Jornet[(2)], Arjun Singh[(3)], and Arjuna Madanayake[(1)]
[(1)] Florida International University, Miami, FL, [(2)] Northeastern University, Boston, MA,
[(3)] SUNY Polytechnic Institute, Utica, NY, USA
{bgaya003, amadanay}@fiu.edu, singha8@sunypoly.edu, j.jornet@northeastern.edu

***Abstract*—The D-band (110-170 GHz) is an ideal candidate to address increasing demand in high-speed wireless communication due to its abundant spectrum. Within this 60 GHz band, there are restricted segments, which require high-precision filter responses adhering to regulatory bounds. Additionally, software defined radio (SDR)-based D-band communications that exploit the available bandwidth while complying to spectral mask requirements using real-time Digital Signal Processors (DSPs) are challenging to realize. We demonstrate the ability to sample and process two channels at 64 GS/s, through multi-rate channelization on the digital side. We show digital mixer-based frequency selection of a 4 GHz sub-band anywhere within 0-32 GHz using Intel Altera Stratix-10 AX chiplet platform. The paper is a novel demonstration on the feasibility of 128-phase multirate systolic array processors to process up to 64 GHz of passband in real-time using an Altera FPGA core.**

***Index Terms*—Bandwidth, Chiplet, D-band, DSP, Intel.**

I. Introduction

High-capacity wireless systems exploiting the spectrum in the sub-THz bands (100-300 GHz) have the luxury of abundant bandwidth [1], [2]. The D-band (110-170 GHz), for example, has up to 60 GHz of bandwidth. However, there are technical and regulatory challenges for using this bandwidth for communications. A sub-THz software defined radio (SDR) must process the 60 GHz baseband in real-time using a DSP [3], [4]. There are licensing requirements to allow for scientific, government and other uses depending on the area of use, directions of wave propagation, and the allowable harmful interference to protected systems. Control of the baseband processor is crucial for ensuring efficient DSP functionality as well as compliance to regulations.

II. D-band Front-End and SDR Backend

Fig. 1 (a) system architecture of the 135–150 GHz RF front-end and DSP, enabling 64 GS/s. The RF front end consists of an up-converter unit (UCU), a power amplifier (PA), and a down-converter unit (DCU) from Virginia Diodes Incorporated (VDI). A 135–150 GHz bandpass filter sets allowable spectral range. The UCU includes an amplifier followed by a mixer with a 10 dB conversion loss, while the transmitter and receiver incorporates high-gain lens antennas (40 dBi) in the far-field region [5], [6].

A. ADC/DAC at 64 GS/s

The Intel Stratix-10 AX system on chip (SoC) field programmable logic array (FPGA) has integrated data converters with sampling rates of upto 64 GS/s utilizing 14 nm complementary metal oxide semiconductor (CMOS) technology. It has 2 A-Tile Direct-RF transceivers that can operate up to 64 GS/s, while the development board provides full access to 8 analog to digital converters (ADCs) and 8 digital to analog converters (DACs). Due to the chiplet interconnects being limited in capacity, each ADC/DAC can handle 4 GS/s at a time when all 8 ports are used. When two channels in each A-tile, specifically *port0* and *port1* are active, the system can achieve an effective sample rate of 8 GS/s per channel. We use a sample rate of 8 GS/s per ADC/DAC, which allows IQ bandwidths of 8 GHz (bandpass) per pair of channels.

In the A-Tile architecture, an ADC is configured with a coarse Digital Downconverter (DDC), followed by up to four fine DDCs. The DAC is set up with four fine Digital Upconverters (DUCs) and a coarse DUC. Each port incorporates a Numerically Controlled Oscillator (NCO), which can be programmed to adjust the parameters for specific decimation and interpolation modes. The ADCs and DACs employ a pipelined architecture with interleaving, enabling them to achieve high sampling rates and resolution. Furthermore, calibration algorithms for both ADCs and DACs are integrated in the A-Tile to optimize RF performance.

B. FPGA Programmability

Quartus Prime Pro provides the A-Tile Direct RF-XCVR soft IP to configure the ADC/DACs, and an interface to control A-tile reference clocking. We use a pre-loaded sampling rate from 12 clock frequency options, ranging between 40-64 GS/s. The tuning of the NCO that performs mixer functionality in the digital domain is performed at runtime through customized Tool Command Language (TCL) scripts.

III. Experimental Setup

The goal is to process D-band range in a DSP processor. We demonstrate in-phase (I)/quadrature (Q) sampling at 64 GS/s per channel, resulting in 64 GHz at intermediate frequency (IF) using two channels. The 32 GHz I/Q channels are channelized across 4 GHz chunks per ADC/DAC pair, with decimation factor of 8 within the Altera FPGA. Eight parallel 4 GHz channels are combined to get 32 GHz, with FPGA operating at 250 MHz across 128 parallel polyphase channels.

A. DSP Architecture for 64 GHz-Wide IQ-Baseband

The use of 128 parallel streams on the FPGA allows massively parallel computing functions. Systolic arrays are

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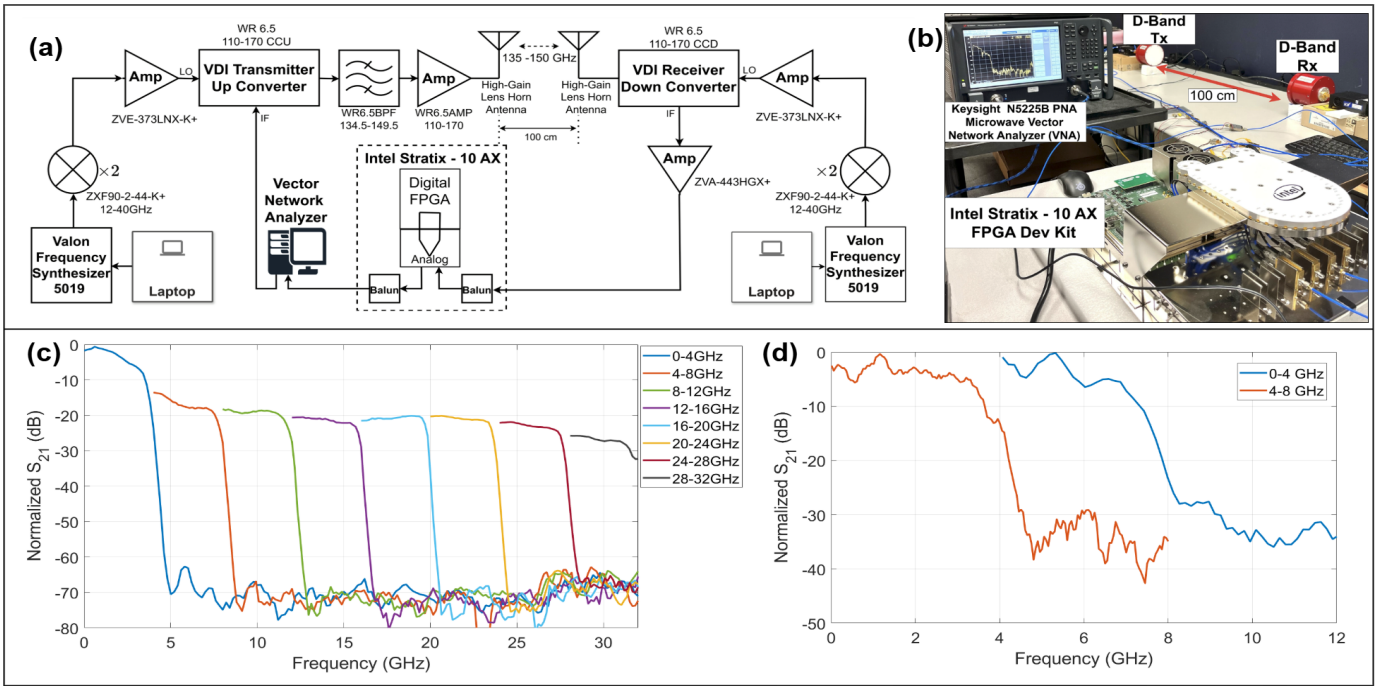

Fig. 1. (a) Test schematic, (b) Stratix-10 AX FPGA with D-band front end, (c) S_{21} of 4 GHz bands across 0-32 GHz processed in polyphase inside Stratix-10 AX FPGA (normalized), (d) S_{21} of Tx+Channel+Rx+ADC+FPGA+DAC path measured for 0-4 GHz and 4-8 GHz bands (normalized).

locally interconnected, modular, and regular. Systolic arrays maximally utilize compute capability as there is no serially executed code (Ahmdahl's Law). The design exemplifies sampling, polyphase channelization (analysis) and DAC (synthesis), across 128 channels. Eventually, we will use a maximally-decimated uniform-DFT polyphase filterbank for the analysis section to carve out the continuous bands within 110-170 GHz.

B. RF-Test Setup and the Experimental Outcomes

The channelization of 4 GHz chunks from the 32 GHz of RF bandwidth from one ADC port (*port0*) is demonstrated by measuring S_{21} across ADC-FPGA-DAC path. The test ports 1 and 2 of a Keysight N5225B PNA Microwave Vector Network Analyzer (VNA) (10 MHz–50 GHz) are calibrated to 50 ohms over the 0–32 GHz range for frequency response measurements as illustrated in Fig. 1 (c). The output power of VNA is set at -5 dBm feeding the ADC of the FPGA. The VNA start frequency is set from 0 to 32 GHz in 4 GHz intervals for each measurement, while the NCO center frequency (CF) is adjusted to match each starting frequency.

As depicted in Fig. 1 (b), the S_{21} of the Tx-Channel-Rx-ADC-FPGA-DAC path is measured across 1 m air gap. The VNA is calibrated for two frequency bands: 0–8 GHz and 4–12 GHz, with the NCO CF set to 0 Hz and 4 GHz, respectively. The normalized measurements are in Fig. 1 (d). The LO is configured to transmit signals within the 140–148 GHz band. Similarly, by adjusting the NCO CF accordingly, our testbed can process any 4 GHz of bandwidth at runtime across the entire 0–32 GHz RF band per channel.

IV. Conclusion

DSP with 64 GHz baseband on Stratix-10 AX chiplets was demonstrated as pass-through pipes. Real-time demo has a D-band system, an ADC, a DAC, and an FPGA, in the loop. Full SDR functionality with 64 GHz bandwidth is an ongoing work.

Acknowledgements

Authors thank NSF, NIST and AFRL for partial support.

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